L&T Technology Services

FPGA: DEQEL –TESTING SYSTEM FOR MULTIPLE DUTS.

PROJECT SCOPE

- Concurrent Testing of 80 ASIC Over Temperature Range of -25C up to +150C
- 80 Parallel Tested Duts.
- Non-standard PCB Material
- Signal and Routing Challenges – Density and Length
- Xilinx Virtex Ultrascale