

IMAGE PROCESSING: TURNKEY SOC

WHAT WE DID

- // Complete physical design and verification of image processing SoC
- // Executed the chip plans, SoC plans, and IT plans using low power process methodology
- // Attained processing efficiency of the highest level with calculations for the die size, pin count, and power/memory/performance/sensor requirements

KEY HIGHLIGHTS

- // 5 Million Gates With 400+ Macros
- // 40+ Image Processing Algorithms
- // Sensor Interface
- // Parallel Image Interface
- // GigE Vision Compatibility
- // 5+ Clock Domains With Maximum Frequency of 800Mhz
- // Full Chip Verification Environment