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(71) Applicant(s): L&T TECHNOLOGY SERVICES LIMITED

(72) Inventor(s): SUBASH, D

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(54) Title: A CLOSED LOOP CONTROL METHODOLOGY FOR MODIFIED SEPIC DC/DC CONVERTER

(57) Abstract: The invention relates to a method and system for providing a design of a combined closed loop ANFIS voltage controller and Hysteresis current controller for modified SEPIC DC/DC converter. The ANFIS based voltage controller and Hysteresis current controller are used together to form a closed loop controller that increases the output regulation of the controller and also the power quality in terms of THD, input power factor, peak overshoot time and settling time.

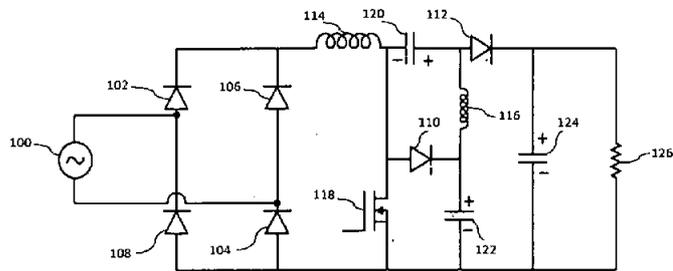


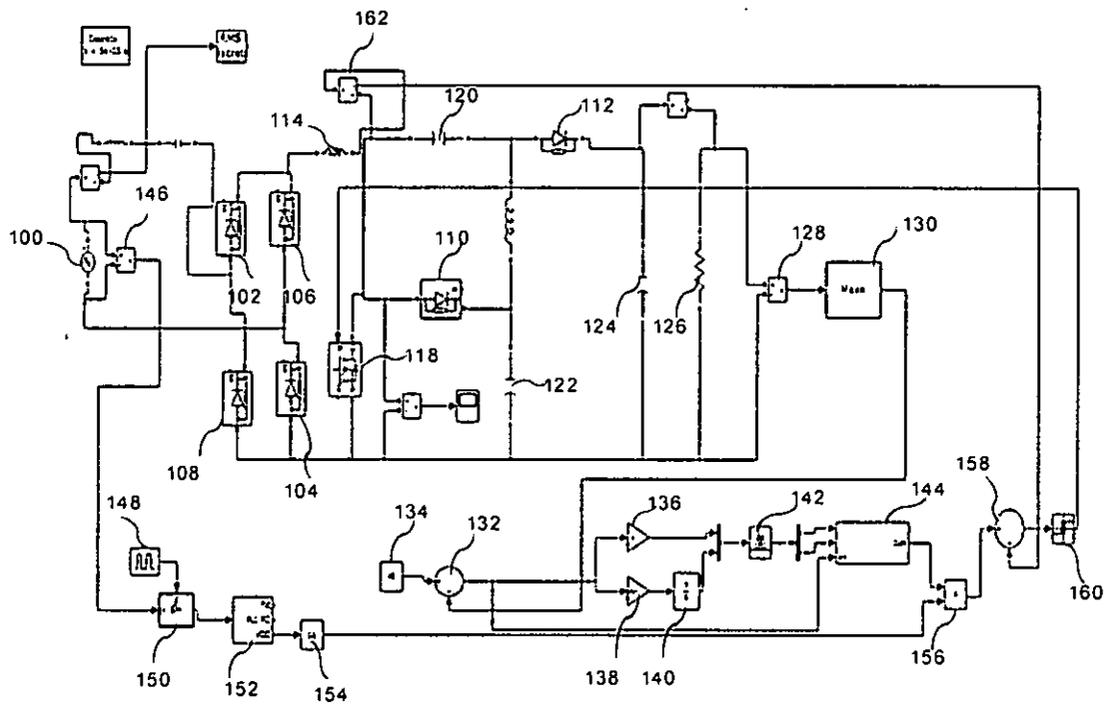
Figure 1



ABSTRACT

A Closed Loop Control Methodology for Modified SEPIC DC/DC Converter

The invention relates to a method and system for providing a design of a combined closed loop ANFIS voltage controller and Hysteresis current controller for modified SEPIC DC/DC converter. The ANFIS based voltage controller and Hysteresis current controller are used together to form a closed loop controller that increases the output regulation of the controller and also the power quality in terms of THD, input power factor, peak overshoot time and settling time.



23-Mar-2018/225113/201741010411/Abstract

We Claim:



1. A system for improving performance of a DC to DC power converter, the system comprising:
 - a modified single-ended primary-inductor converter (SEPIC) DC to DC converter;
 - an adaptive network-based fuzzy inference system (ANFIS) voltage controller; and
 - a hysteresis current controller;wherein the ANFIS voltage controller and the hysteresis current controller form a closed loop controller for the modified SEPIC DC to DC converter.
2. The system as claimed in claim 1, wherein the performance is measured in terms of power quality.
3. The system as claimed in claim 2, wherein the power quality is measured in terms of total harmonic distortion (THD), input power factor, peak overshoot time and settling time.

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Mohammed Faisal (INPA No: 1941)
Head, IPR Dept.
L&T Technology Services Limited
DLF 3rd Block, 2nd Floor,
Manapakkam, Chennai, TN, 600089

23-Mar-2018/22513/201741010411/Claims



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FIELD OF INVENTION

The invention generally relates to system and methods for improving power quality in DC/DC converters and more particularly to improving power quality for modified SEPIC DC/DC converters.

BACKGROUND

In conventional DC/DC converters, the power quality is low which results in heavy losses. In order to avoid losses, a control system is required in DC/DC converters. Some of the existing control systems for power output of DC/DC converters includes Proportional Integral (PI) controller, Fuzzy Logic controller, fuzzy tuned PI controller, ANFIS controller and Hysteresis controller.

In Proportional Integral (PI) controller, proportional control action tends to stabilize the converter system, while the integral control action tends to eliminate or reduce steady-state error in response to various inputs. However, using PI controller results in higher total harmonic distortion (THD) and increased peak overshoot.

In Fuzzy Logic controller, fuzzy logic is used. Fuzzy logic is a set of mathematical principles for knowledge representation and reasoning based on degrees of membership. It is the logic underlying approximate, rather than exact, modes of reasoning. The THD is less than the PI controller but the peak overshoot is still more when using this controller.

In fuzzy tuned PI controller, the manual tuning of controller is eliminated. Here, the output scaling factor (SF) is adjusted online by fuzzy rules according to the current trend of the controlled process. The peak overshoot is reduced in fuzzy tuned PI controller but still the voltage THD is more.

Adaptive neuro-fuzzy inference system (ANFIS) control is a combination of fuzzy logic control and neural networks. The ANFIS structure model has five layers namely input layer, input membership function, rules, output membership function and output. The basic logical operation is used to create the rules.

Hysteresis controller is used for improving the power factor in converters and reduce the ripples in output waveform. The controller can accept or reject the disturbances within a hysteresis band since the loop never reaches quiescent state. The error value in hysteresis band should not be zero.

Single-ended primary inductor converter (SEPIC) converter is a buck-boost converter. The switch voltage of SEPIC converter is the sum of output voltage and input voltage. Therefore the voltage stress on the switch will be more. The conventional SEPIC suffers from high switching losses. In order to overcome this problem, additional multiplier diode and multiplier capacitor are included in the configuration of the conventional SEPIC converter which is called as modified SEPIC converter.

The above mentioned controllers suffer from their own drawbacks. Thus, a new design with a closed loop control methodology is needed for the DC/DC converters that can improve the power quality and avoid losses. The design includes a combined closed loop ANFIS voltage

controller and hysteresis current controller for modified SEPIC DC/DC converter to improve power quality.

The present invention is directed to overcoming one or more of the problems as set forth above.

SUMMARY OF THE INVENTION

Exemplary embodiments of the invention disclose a method and system for providing a design of a combined closed loop ANFIS voltage controller and Hysteresis current controller for modified SEPIC DC/DC converter. The ANFIS based voltage controller and Hysteresis current controller are used together to form a closed loop controller that increases the output regulation of the controller and also the power quality in terms of THD, input power factor, peak overshoot time and settling time.

BRIEF DESCRIPTION OF DRAWINGS

Other objects, features, and advantages of the invention will be apparent from the following description when read with reference to the accompanying drawings. In the drawings, wherein like reference numerals denote corresponding parts throughout the several views:

Figure 1 illustrates a circuit diagram of a modified SEPIC DC/DC converter, according to an exemplary embodiment of the invention;

Figure 2 illustrates a circuit diagram for first mode of operation of the modified SEPIC DC/DC converter, according to an exemplary embodiment of the invention;

Figure 3 illustrates a circuit diagram for second mode of operation of the modified SEPIC DC/DC converter, according to an exemplary embodiment of the invention;

Figure 4 illustrates a circuit diagram for modified SEPIC DC/DC converter with ANFIS voltage controller and Hysteresis current controller, according to an exemplary embodiment of the invention;

Figure 5 illustrates input voltage and input current waveforms of modified SEPIC DC/DC converter with ANFIS voltage controller and Hysteresis current controller;

Figure 6 illustrates output voltage waveforms of modified SEPIC DC/DC converter with ANFIS voltage controller and Hysteresis current controller; and

Figure 7 illustrates a table showing comparison between existing controllers for modified SEPIC DC/DC converter and combination of ANFIS voltage controller and Hysteresis current controller for modified SEPIC DC/DC converter.

DETAILED DESCRIPTION OF DRAWINGS

The following description with reference to the accompanying drawings is provided to assist in a comprehensive understanding of exemplary embodiments of the invention. It includes various specific details to assist in that understanding but these are to be regarded as merely exemplary. Accordingly, those of ordinary skill in the art will recognize that various changes and modifications of the embodiments described herein can be made without departing from the scope and spirit of the invention. In addition, descriptions of well-known functions and constructions are omitted for clarity and conciseness.

FIG. 1 illustrates a circuit diagram of a modified SEPIC DC/DC converter, according to an exemplary embodiment of the invention. The circuit includes AC voltage source 100, diodes 102, 104,

106, 108, 110 and 112, inductors 114 and 116, capacitors 120, 122 and 124, transistor 118 and resistor 126. The AC voltage source 100, diodes 102, 104, 106, 108 and 112, inductor 114 and 116, transistor 118, capacitors 120 and 124, resistor 126 form the conventional SEPIC converter. The addition of diode 110 and capacitor 122 to the conventional SEPIC converter makes the circuit to a modified SEPIC converter.

The modified SEPIC converter may operate in two modes. The first mode of operation of modified SEPIC converter is illustrated in Figure 2 and the second mode of operation of the modified SEPIC converter is illustrated in Figure 3.

The terms DC/DC converter and DC to DC converter may be used interchangeably.

Figure 2 illustrates the first mode of operation of modified SEPIC DC/DC converter. According to an embodiment, at the instant t_0 , the switch 118 is turned-off. Hence, the energy stored in the input inductor 114 is transferred to the output through the capacitor 120 and output diode 112. The energy stored in the input inductor 114 is transferred to capacitor 122 through the diode 110. Therefore, the switch 118 voltage is equal to the capacitor 122 voltage. The energy stored in the inductor 116 is transferred to the output through the diode 112.

FIG. 3 illustrates the second mode of operation of modified SEPIC DC/DC converter. According to an embodiment, at the instant t_1 , the switch 118 is turned-on. Hence, the diodes 110 and 112 are blocked and the inductors 114 and 116 store energy. The input voltage is applied to the input inductor 114 and the voltage difference between capacitors 120 and 122 is applied to the inductor 116. The resultant voltage is higher than the voltage of capacitor 120.

According to an embodiment, the voltage applied to the inductor 116 during the conduction of the power switch 118 is higher than that in the conventional SEPIC, thereby increasing the static gain.

FIG. 4 illustrates the circuit diagram of modified SEPIC DC/DC converter with ANFIS voltage controller and Hysteresis current controller, according to an embodiment of the invention.

The terms 'adaptive neuro-fuzzy inference system' and 'adaptive network-based fuzzy inference system' may be used interchangeably for ANFIS.

The mean output voltage 130 from the modified SEPIC DC/DC converter is fed to a comparing circuit 132. The comparing circuit 132 compares the mean output voltage 130 with a constant 134. The difference in the output voltage value is fed to two comparators 136 and 138. The output voltage from comparator 138 is fed to an integrator circuit 140. The output from comparator 136 and output from integrator 140 is fed to an ANFIS controller 142. Multiple outputs from ANFIS controller and output from comparing circuit 132 is fed to a multiple input single output (MISO) system 144.

As illustrated in Figure 4, the source voltage 146 is fed to a sampling and holding circuit 150. Clock pulse 148 is also fed to the sampling and holding circuit 150. The resultant sampled voltage is fed to a phase locked loop system 152. The absolute value of voltage from modulus circuit 154 is fed to a multiplier circuit 156. The output from MISO 144 is also fed to the multiplier circuit 156. The resultant voltage from the multiplier circuit 156 is fed to a summing circuit 158. The input current from current measuring instrument 162 is also fed to the summing circuit 158.

The output from the summing circuit 158 is fed to a relay switch 160. The resultant value from the relay switch is finally fed to the switch 118 for determining the turning ON and OFF of the switch 118.

The process as explained in Figure 4 from mean output voltage 130 is repeated in a closed loop manner that determines the state of the switch 118.

Figure 5 illustrates input voltage and input current waveforms of modified SEPIC DC/DC converter with combination of ANFIS voltage controller and Hysteresis current controller.

Figure 6 illustrates output voltage waveform of modified SEPIC DC/DC converter with combination of ANFIS voltage controller and Hysteresis current controller. As seen in Figure 6, there is no peak overshoot in the output voltage.

Figure 7 illustrates a table showing comparison between existing controllers for modified SEPIC DC/DC converter and combination of ANFIS voltage controller and Hysteresis current controller for modified SEPIC DC/DC converter. From Figure 7, conclusion may be inferred that THD percentage and settling time for modified SEPIC DC/DC converter with combination of ANFIS voltage controller and Hysteresis current controller is very less as compared to existing controllers. However, the power factor has improved as compared to the existing controllers and the value of power factor is 0.9997 which is close to unity. Also, there is no peak overshoot in the output voltage when combination of ANFIS voltage controller and Hysteresis current controller is used with modified SEPIC DC/DC converter.

The modified SEPIC DC/DC converter with combination of ANFIS voltage controller and Hysteresis current controller may result in less failure of industrial devices and provides efficient operation of high voltage and high current devices.

In the drawings and specification there has been set forth preferred embodiments of the invention, and although specific terms are employed, these are used in a generic and descriptive sense only and not for purposes of limitation. Changes in the form and the proportion of parts, as well as in the substitution of equivalents, are contemplated as circumstances may suggest or render expedient without departing from the spirit or scope of the invention.

Throughout the various contexts described in this disclosure, the embodiments of the invention further encompass computer apparatus, computing systems and machine-readable media configured to carry out the foregoing systems and methods. In addition to an embodiment consisting of specifically designed integrated circuits or other electronics, the present invention may be conveniently implemented using a conventional general purpose or a specialized digital computer or microprocessor programmed according to the teachings of the present disclosure, as will be apparent to those skilled in the computer art.

Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will be apparent to those skilled in the software art. The invention may also be implemented by the preparation of application specific integrated circuits or by interconnecting an appropriate network of conventional component circuits, as will be readily apparent to those skilled in the art.

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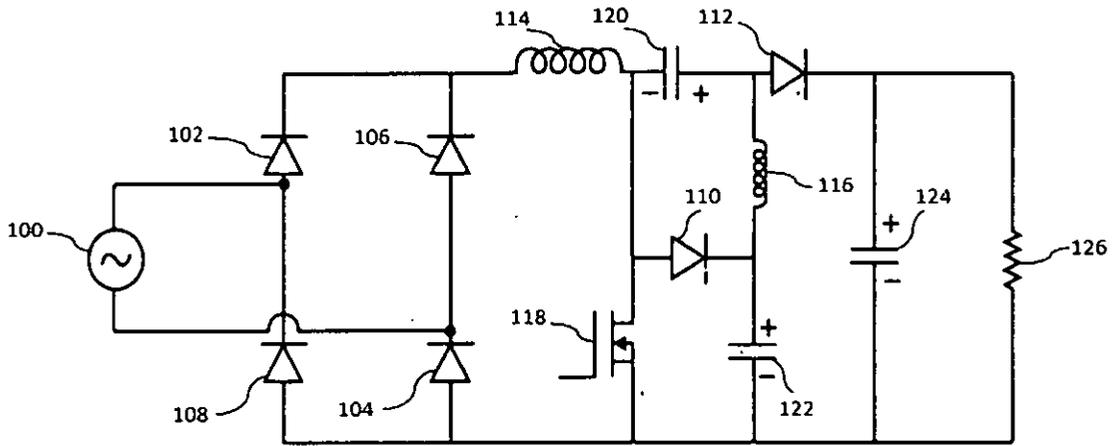
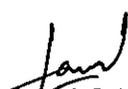


Figure 1


Mohammed Faisal (INPA No: 1941)
Head, IPR Dept.
L&T Technology Services Limited
DLF 3rd Block, 2nd Floor,
Manapakkam, Chennai – 600089

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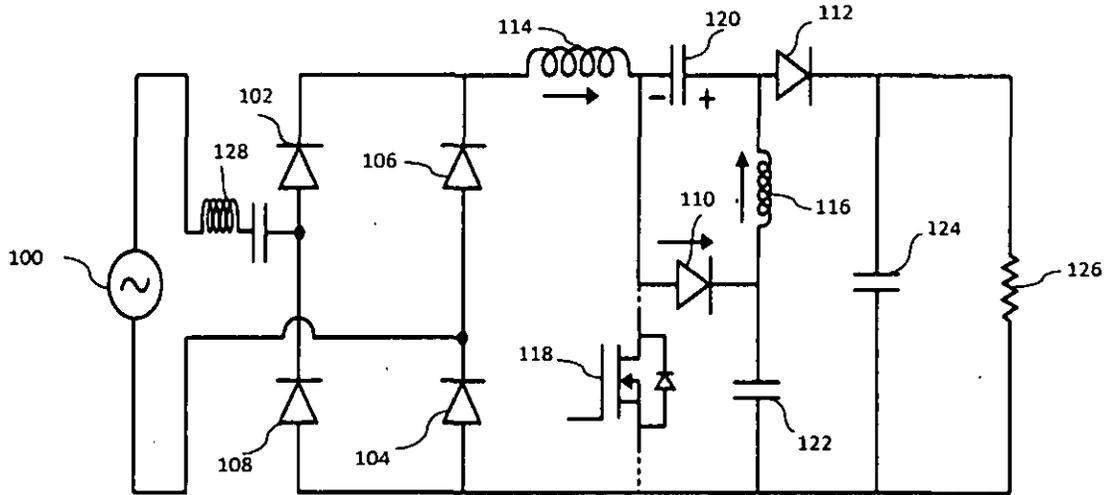


Figure 2


Mohammed Faisal (INPA No: 1941)
Head, IPR Dept.
L&T Technology Services Limited
DLF 3rd Block, 2nd Floor,
Manapakkam, Chennai – 600089

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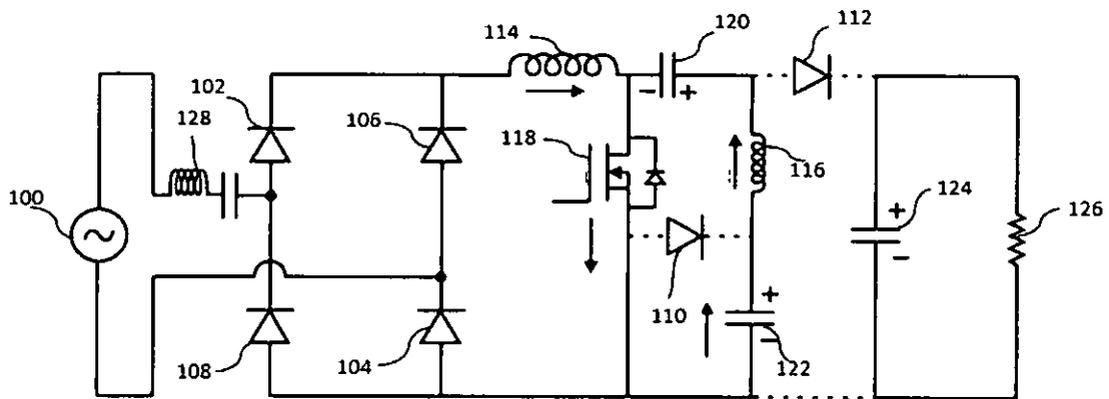


Figure 3

Faisal
Mohammed Faisal (INPA No: 1941)
Head, IPR Dept.
L&T Technology Services Limited
DLF 3rd Block, 2nd Floor,
Manapakkam, Chennai – 600089

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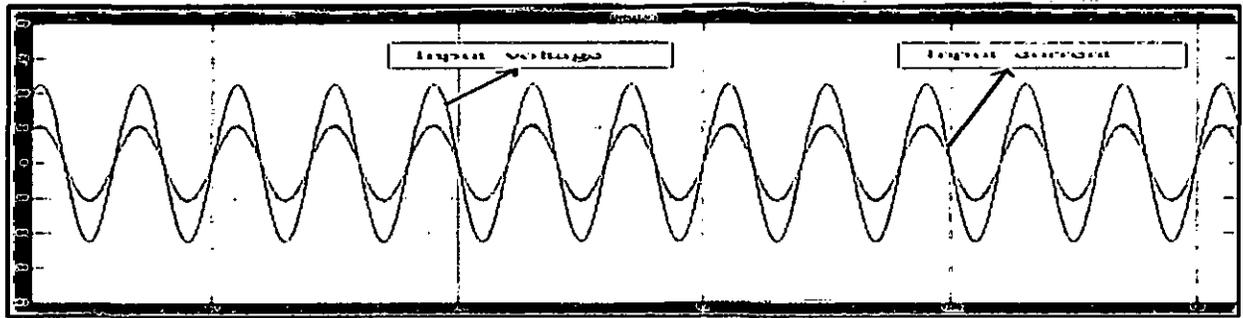
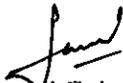


Figure 5


Mohammed Faisal (INPA No: 1941)
Head, IPR Dept.
L&T Technology Services Limited
DLF 3rd Block, 2nd Floor,
Mallapakkam, Chennai - 600089

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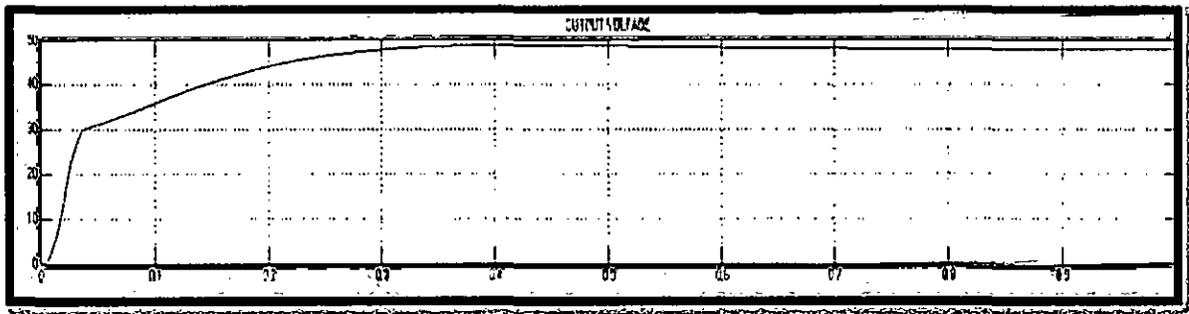


Figure 6

Mohammed Faisal (INPA No: 1941)
Head, IPR Dept.
L&T Technology Services Limited
DLF 3rd Block, 2nd Floor,
Manapakkam, Chennai - 600089

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Controller	THD (%)	Power Factor	Peak Overshoot (%)	Settling time (s)
PI voltage controller and PI current controller	7.39	0.9972	12.5	1.5
Fuzzy voltage controller and Hysteresis current controller	4.15	0.9986	5	1
Fuzzy tuned PI voltage controller and hysteresis current controller	3.93	0.9991	2	0.8
ANFIS voltage controller and hysteresis current controller	1.39	0.9997	No peak overshoot	0.35

Figure 7


Mohammed Faisal (INPA No: 1941)
Head, IPR Dept.
L&T Technology Services Limited
DLF 3rd Block, 2nd Floor,