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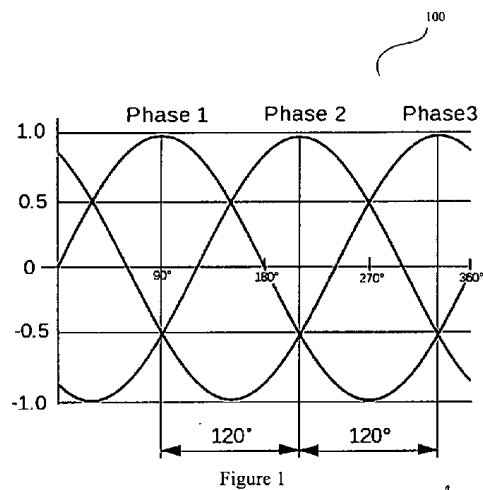
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(54) Title: PHASE SEQUENCE DETECTION IN THREE PHASE POWER SYSTEM

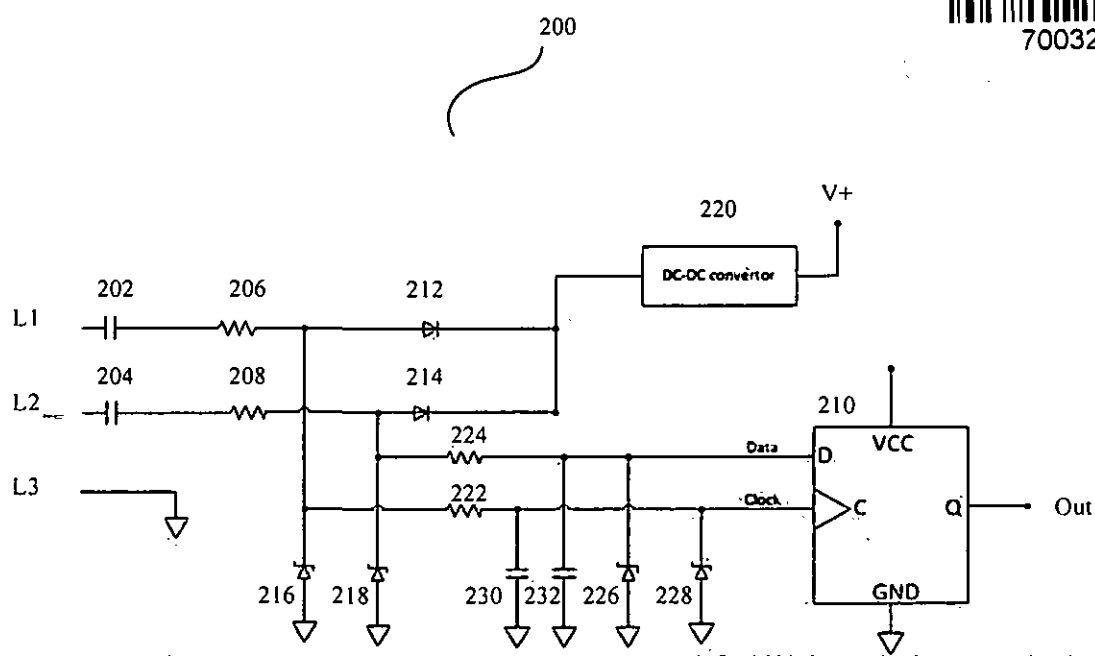
(57) Abstract: According to embodiments of the invention, a phase sequence detection arrangement for a three phase three wire AC power system is disclosed. The disclosed system includes a first conductor (L1), a second conductor (L2) and a third conductor (L3) such that each conductor (L1, L2, L3) carries alternating current (AC) of same frequency and voltage amplitude and with a phase difference, a single D flip flop circuit (210) connected to the first conductor (L1) and the second conductor (L2) in series for detecting if phase in the conductors (L1, L2, L3) is in sequence or not; and a DC power supply for providing an input voltage to the D flip flop circuit (210); wherein the Output of the D flip flop (210) is a control signal that may detect phase sequence of the three phase three wire AC.



Abstract

Phase Sequence Detection in Three Phase Power System

According to embodiments of the invention, a phase sequence detection arrangement for a three phase three wire AC power system is disclosed. The disclosed system includes a first conductor (L1), a second conductor (L2) and a third conductor (L3) such that each conductor (L1, L2, L3) carries alternating current (AC) of same frequency and voltage amplitude and with a phase difference, a single D flip flop circuit (210) connected to the first conductor (L1) and the second conductor (L2) in series for detecting if phase in the conductors (L1, L2, L3) is in sequence or not; and a DC power supply for providing an input voltage to the D flip flop circuit (210); wherein the Output of the D flip flop (210) is a control signal that may detect phase sequence of the three phase three wire AC.



FIELD OF INVENTION

The invention relates to three phase power systems and, more particularly, to phase sequence detection in three phase power systems.



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BACKGROUND

Incorrect phase sequence within a three-phase power system is called phase reversal. Phase reversal usually occurs due to mistakes made during equipment installation, maintenance, or modifications to the facility power system.

When the phase sequence of a three-phase system is incorrect, the connected three-phase motors and other rotating equipment runs in the opposite direction. In many cases, this can cause a hazardous condition that may destroy product, damage machinery, and injure personnel.

Existing solutions for phase sequence detection are either dependent on software or include more number of hardware components. Hence, there is a need for developing a method for phase sequence detection that is not dependent on software and includes minimum number of hardware components, thereby minimizing the cost.

The present invention is directed to overcoming one or more of the problems as set forth above.

SUMMARY OF THE INVENTION

Exemplary embodiments of the invention disclose a circuit for phase sequence detection of a three phase three wire AC power system. The phase sequence detection circuit monitors a three phase AC sequence and provides an output indicative of phase sequence of the three

phases. According to an embodiment, the circuit includes a single D flip flop for detecting if phase is in sequence or not. Output of the D flip flop is a control signal that detects phase sequence of three phase AC. According to an embodiment, the control signal output may be low or high. According to an exemplary embodiment, the control signal may be high if phases of the three phase AC input are in sequence and low if phases of the three phase AC input are not in sequence.

BRIEF DESCRIPTION OF DRAWINGS

Other objects, features, and advantages of the invention will be apparent from the following description when read with reference to the accompanying drawings. In the drawings, wherein like reference numerals denote corresponding parts throughout the several views:

Figure 1 illustrates pulse waveforms of a three phase AC power system, according to an embodiment of the invention;

Figure 2 shows a phase sequence detection circuit of a three phase three wire AC power system, according to an exemplary embodiment of the invention;

Figure 3 shows pulse waveforms of a phase sequence detector when three phases of a three phase three wire AC power system are in phase, according to an exemplary embodiment of the invention; and

Figure 4 shows pulse waveforms of a phase sequence detector when three phases of a three phase three wire AC power system are out of phase, according to an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF DRAWINGS

The following description with reference to the accompanying drawings is provided to assist in a comprehensive understanding of exemplary embodiments of the invention. It includes

various specific details to assist in that understanding but these are to be regarded as merely exemplary. Accordingly, those of ordinary skill in the art will recognize that various changes and modifications of the embodiments described herein can be made without departing from the scope and spirit of the invention. In addition, descriptions of well-known functions and constructions are omitted for clarity and conciseness.

According to embodiments of the invention, a circuit for a phase sensitive detector is disclosed.

Figure 1 illustrates a pulse waveform of a three-phase alternate current (AC) power system, according to an embodiment of the invention. The three phase AC power system includes three conductors and each conductor carries AC of same frequency and voltage amplitude relative to a common reference. However, the three conductors have a phase difference of one third of a cycle between each of the three conductors. Due to the phase difference, voltage on any conductor reaches its peak value at one third of a cycle after one of the other conductors and one third of a cycle before the remaining conductor.

The three AC lines namely Line 1(L1), Line 2 (L2) and Line 3 (L3) shown in Figure 1 represent phase 1, phase 2 and phase 3 respectively. The phase difference between the three lines L1, L2 and L3 is uniform and each phase reaches peak value in one third of a cycle. The phase 1(Line 1) reaches peak first, phase 2(Line 2) follows phase 1(Line 1) and phase 3(Line 3) follows phase 2(Line 2).

Figure 2 shows a phase sequence detection arrangement/circuit of the three phase three wire AC power system, according to an embodiment of the invention. The phase sequence detection

arrangement/circuit monitors the three phase three wire AC sequence and provides an output indicative of the phase sequence of the three phases.

In Figure 2, Line 1(L1), Line 2 (L2) and Line 3 (L3) correspond to phase1, phase2 and phase3 respectively of the three phase three wire AC power system. According to an embodiment, the lines L1, L2 and L3 may be identified by a predefined color code. The color codes of lines L1, L2 and L3 may vary depending on various factors such as legal requirements prescribed by a specific country.

A first capacitor (202) may be connected in series with a first resistor (206) to provide impedance for the Line1 and a second capacitor (204) may be connected in series with a second resistor (208) to provide impedance for the Line2. The impedance for Line1 and Line2 may be required to produce appropriate voltage for a single D flip flop (210) circuit connected to the Line 1 & Line 2. A voltage drop may occur across the capacitors (202, 204) and remaining voltage may be fed to a bridge rectifier comprising of plurality of a first diode (212), a second diode (214), a third diode (216) and a fourth diode (218).

According to an embodiment, the third diode (216) and the fourth diode (218) may be Zener diodes. The breakdown value of the third and fourth diodes (216, 218) depends on the voltage that needs to be provided as input to a DC power supply. The output of the DC power supply provides a supply voltage needed for the D flip flop (210). The D flip flop (210) may have a data input, a clock input and a logic output.

According to embodiments of the invention, the combination of the capacitors (202, 204), the resistors (206, 208) and the diodes (212, 214, 216, 218) may be used to generate a wave shaped signal from the AC input and provide the wave shaped input to the D flip flop (210).

According to yet another embodiment, a DC to DC converter (220) may be used to convert the voltage generated from the Lines (L1, L2 and L3) to appropriate voltage required for the D flip flop (210). According to an embodiment, an external voltage source may be used in place of a DC to DC converter.

According to an exemplary embodiment an another set of resistors (222, 224) and diodes (226, 228) may be used to further reduce the voltage generated by the bridge rectifier. According to another exemplary embodiment, the resistor (222, 224), the diodes (226, 228) may not be required in the phase sequence detection circuit.

According to yet another embodiment, an another set of capacitors (230, 232) may be used for decoupling a high frequency noise such as, but not limited to, inductive noise. According to an embodiment, the capacitors (230, 232) may be of lower value as compared to first and second capacitors (202, 204). According to an exemplary embodiment, the capacitors (230, 232) may not be required in the phase sequence detection circuit.

According to an exemplary embodiment, the diode (226) may be connected to the clock input of the D flip flop (210) and the diode (228) may be connected to the data input of the D flip flop (210).

Output of the D flip flop (210) is a control signal that may detect phase sequence of the three phase three wire AC. According to an embodiment, the control signal output may be low or high. According to an exemplary embodiment, the control signal may be high if phases of the three phase AC input are in sequence and low if phases of the three phase AC input are not in sequence. According to another embodiment, the control signal may be directly proportional to the phase error in the desired phase relationship between the data pulses and the clock pulses.

According to an embodiment, the output of the D flip flop (210) may be fed as input to other circuits that require status of phase sequence to take further action.

Figure 3 shows pulse waveforms of a phase sequence detector when three phases of a three phase three wire AC power system are in phase, according to an exemplary embodiment of the invention.

L1, L2 and L3 may correspond to phase1, phase2 and phase3 respectively of the three phase three wire system. The Data, Clock and Out correspond to data input, clock input and output of the D flip flop (210) of the phase sequence circuit shown in Figure 2. V+ represent the voltage supplied to the D flip flop (210). Figure 3 illustrates Out is high if L1, L2 and L3 are in phase. If L1, L2 and L3 are in phase, then data input of the D flip flop(210) is defined high during positive transition in clock input.

Out is high if lines L1, L2 and L3 are phased as below:

L1, L2, L3
L3, L1, L2
L2, L3, L1

Figure 4 shows pulse waveforms of a phase sequence detector when three phases of a three phase three wire AC power system are out of phase, according to an exemplary embodiment of the invention. Figure 4 illustrates Out is low if L1, L2 and L3 are not in phase. If L1, L2 and L3 are not in phase, then data input of the D flip flop (210) is defined low during positive transition in clock input.

Out is low if lines L1, L2 and L3 are phased as below:

L2, L1, L3
L3, L2, L1
L1, L3, L2

There are many advantages of the present invention over existing methods for phase sequence detection in a three phase three wire system. The present invention uses only a single flip flop for phase sequence detection. There is no software dependency to determine the phase sequence. The invention is a low cost and effective method for phase sequence detection.

In the drawings and specification there has been set forth preferred embodiments of the invention, and although specific terms are employed, these are used in a generic and descriptive sense only and not for purposes of limitation. Changes in the form and the proportion of parts, as well as in the substitution of equivalents, are contemplated as circumstances may suggest or render expedient without departing from the spirit or scope of the invention.

Throughout the various contexts described in this disclosure, the embodiments of the invention further encompass computer apparatus, computing systems and machine-readable media configured to carry out the foregoing systems and methods. In addition to an embodiment consisting of specifically designed integrated circuits or other electronics, the present invention may be conveniently implemented using a conventional general purpose or a specialized digital

computer or microprocessor programmed according to the teachings of the present disclosure, as will be apparent to those skilled in the computer art.

The embodiments of the present invention may be provided as a computer program product that may include a machine-readable medium, having stored thereon instructions which may be used to program a computer (or other electronic devices) to perform a process according to the present invention. The machine-readable medium may include, but is not limited to, floppy diskettes, optical disks, compact disc read-only memories (CD-ROMs), and magneto-optical disks, ROMs, random access memories (RAMs), erasable programmable read-only memories (EPROMs), electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, flash memory, or other type of media/machine-readable medium suitable for storing electronic instructions. In addition to an embodiment consisting of specifically designed integrated circuits or other electronics, the present invention may be conveniently implemented using a conventional general purpose or a specialized digital computer or microprocessor programmed according to the teachings of the present disclosure, as will be apparent to those skilled in the computer art.

Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will be apparent to those skilled in the software art. The invention may also be implemented by the preparation of application specific integrated circuits or by interconnecting an appropriate network of conventional component circuits, as will be readily apparent to those skilled in the art.



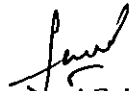
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We Claim:

1. A phase sequence detection arrangement for a three phase three wire AC power system comprising:
 - a first conductor (L1), a second conductor (L2) and a third conductor (L3) such that each conductor (L1, L2, L3) carries alternating current (AC) of same frequency and voltage amplitude and with a phase difference;
 - a single D flip flop circuit (210) connected to the first conductor (L1) and the second conductor (L2) in series for detecting if phase in the conductors (L1, L2, L3) is in sequence or not; and
 - a DC power supply for providing an input voltage to the D flip flop circuit (210);wherein the Output of the D flip flop (210) is a control signal that may detect phase sequence of the three phase three wire AC.
2. The phase sequence detection arrangement as claimed in claim 1, wherein the phase difference in the alternating current (AC) in each conductor is one third of a cycle.
3. The phase sequence detection arrangement as claimed in claim 1, wherein each conductor (L1, L2, L3) identified by a predefined color code.
4. The phase sequence detection arrangement as claimed in claim 1, wherein a first capacitor (202) is connected in series with a first resistor (206) to provide impedance for the current carried in the first conductor (L1) and a second capacitor (204) is connected in series with a second resistor (208) to provide impedance for the current carried in the second conductor (L2).
5. The phase sequence detection arrangement as claimed in claim 4, further comprising a bridge rectifier having a first diode (212), a second diode (214), a third diode (216) and a fourth diode (218).

6. The phase sequence detection arrangement as claimed in claim 5, wherein the third diode (216) and the fourth diode (218) are Zener diodes.
7. The phase sequence detection arrangement as claimed in claim 1, wherein the D flip flop (210) has a data input, a clock input and a logic output.
8. The phase sequence detection arrangement as claimed in claim 1, wherein the DC power supply includes a DC to DC converter (220) to convert the voltage from the conductors (L1, L2 and L3) to the voltage required for the D flip flop (210).
9. The phase sequence detection arrangement as claimed in claim 1, wherein the control signal is high if phases of the three phase AC input are in sequence and low if phases of the three phase AC input are not in sequence.
10. The phase sequence detection arrangement as claimed in claim 7, wherein the control signal is directly proportional to the phase error in the desired phase relationship between the data pulses and the clock pulses.

Dated this 19th day of March 2019


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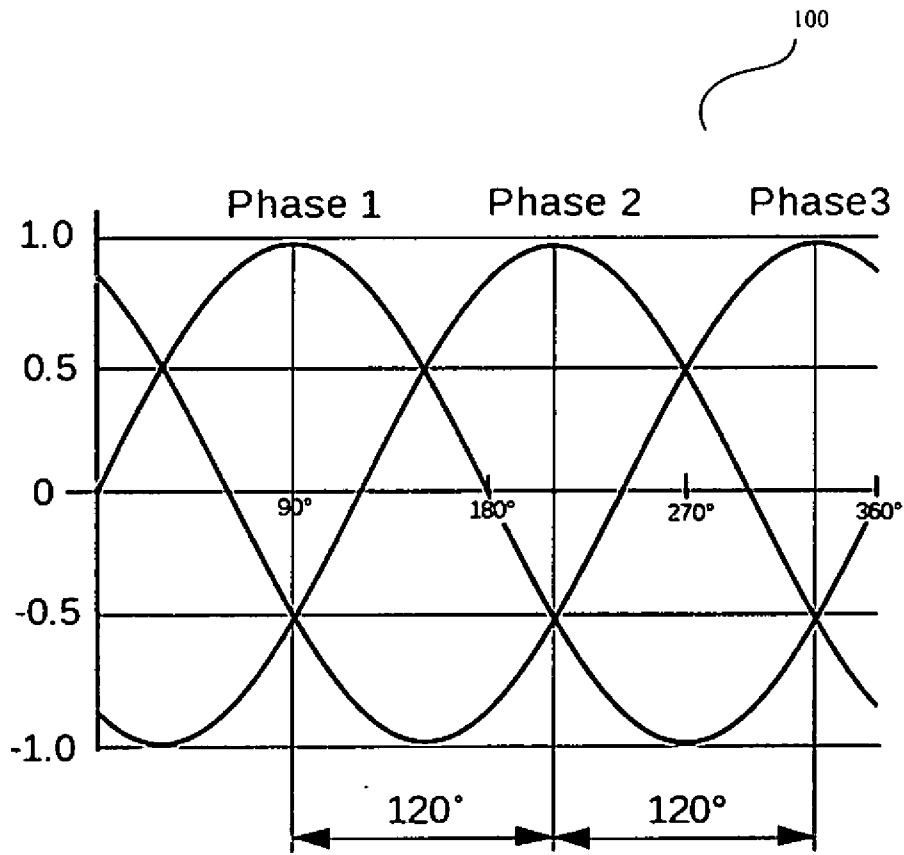


Figure 1

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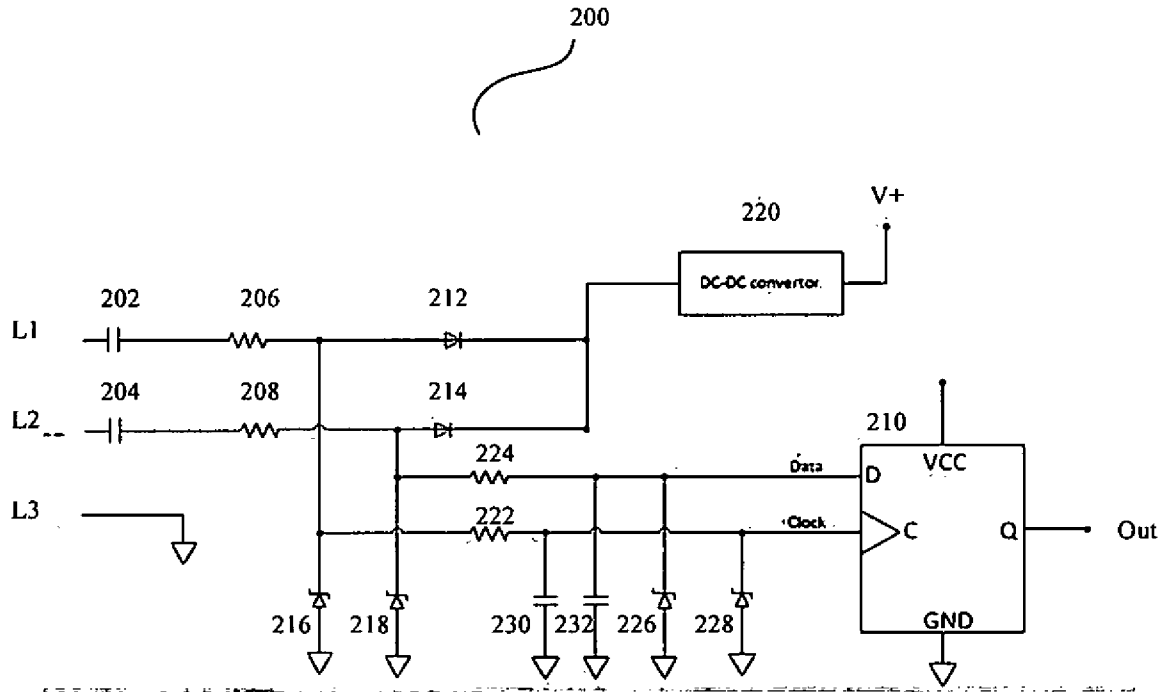


Figure 2

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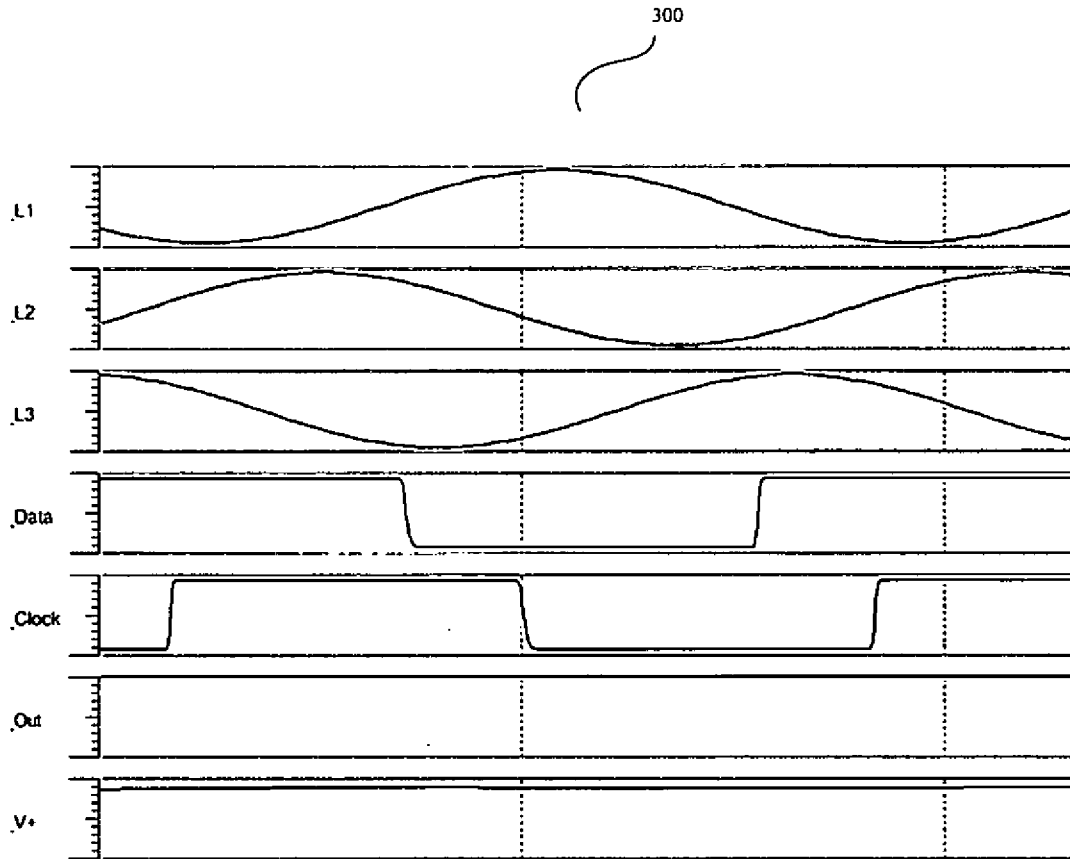



Figure 3


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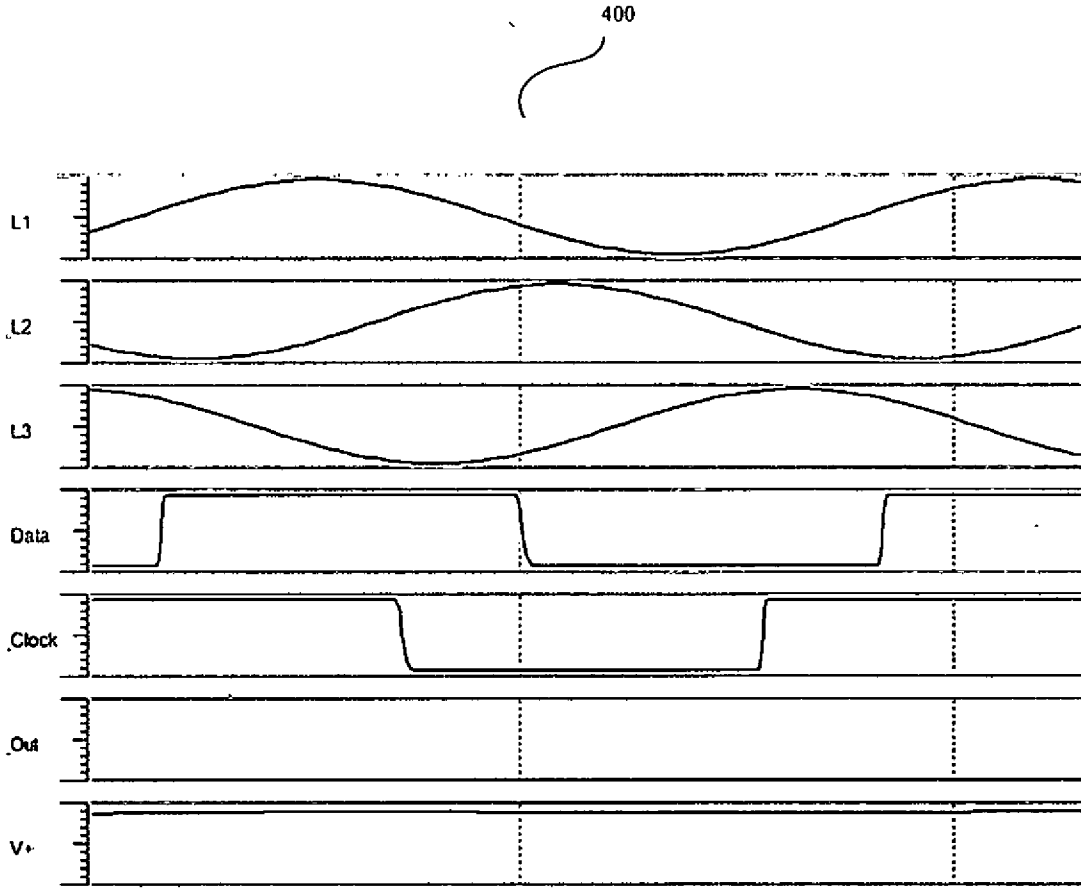



Figure 4


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