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(54) Title: A METHOD AND SYSTEM FOR ANALYSING ELECTRONIC CIRCUIT SCHEMATICS

(57) Abstract: The invention relates to a method and system for analysing electronic circuit schematics in an image format. The method includes converting the electronic circuit schematics into a binary image and forming an image matrix such that all the tracks and components are specified with a specific binary digit and the background is specified in other binary digit, recreating tracks isolating the components, identifying close loop tracks and highlighting the close loop tracks in a predefined color in the image.

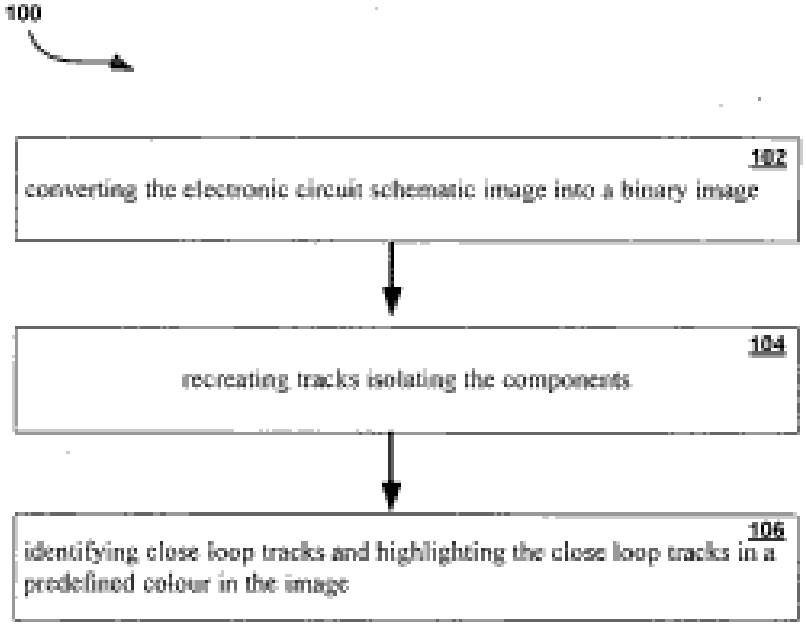

Figure 1

ABSTRACT

The invention relates to a method and system for analysing electronic circuit schematics in an image format. The method includes converting the electronic circuit schematics into a binary image and forming an image matrix such that all the tracks and components are specified with a specific binary digit and the background is specified in other binary digit, recreating tracks isolating the components, identifying close loop tracks and highlighting the close loop tracks in a predefined color in the image.

We Claim:

1. A method of analysing electronic circuit schematics, the electronic circuit schematics being in an image format, the method comprising:

converting the electronic circuit schematic image in a binary image and forming an image matrix such that all the tracks and components are specified with a specific binary digit and the background is specified in other binary digit;

recreating tracks isolating the components; and

identifying close loop tracks and highlighting the close loop tracks in a predefined colour in the image.

2. The method as claimed in claim 1, further comprises, identifying open loop tracks and highlighting the open loop tracks in a predefined colour in the image.

3. The method as claimed in claim 1, further comprises, identifying open loop tracks and the close loop tracks after incorporating components.

4. The method as claimed in any of the preceding claims, wherein the image is in PDF format.

5. The method as claimed in claim 1, further comprises, automatically generating a report of the highlighted close loop tracks.

6. The method as claimed in claim 1, further comprises, generating a reporting highlighting the components and test points on the tracks.

7. The method as claimed in claim 1, wherein the analysing electronic circuit schematics includes DFMEA analysis.

8. The method as claimed in claim 7, wherein the DFMEA analysis is as per MIL-1629A standard.

9. The method as claimed in claim 3, further comprises placing test points for analysing the close loop tracks and components.

10. A system for analysing electronic circuit schematics, the electronic circuit schematics being in an image format, the system comprising:

One or more processors to convert the electronic circuit schematic image into a binary image and forming an image matrix such that all the tracks and components are specified with a specific binary digit and the background is specified in other binary digit;

a recreating component to recreate the tracks after isolating the components; and

a highlighting component to identify close loop tracks and highlight the close loop tracks in a predefined colour in the image.

Dated this 24th day of December 2014

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FIELD OF INVENTION

The invention generally relates to system and methods for analysing electronic circuits and more particularly to detecting circuit tracks and components in schematics of electronic circuits.

BACKGROUND

Circuit diagrams, or schematics, are standard means of representing electronic circuits. While circuit diagrams or schematics is excellent for conveying much of the relevant circuit details in visual form to scientists, engineers and hobbyists, the circuit diagrams or schematics are not able to be readily manipulated or processed by computers.

Having a circuit in computer useable form is required for such applications as automated layout of printed circuit boards, simulating the electrical characteristics of the circuit, and maintaining a database of circuits or circuit modules.

Typically, circuits are subjected to different types or modes of failure. Potential failures may have costly consequences or effects. Hence, it is essential to effectively identify the potential failures and the associated relative risks at an early stage and achieve a better quality product.

Generally, Failure Mode and Effect Analysis (FMEA) may be conducted in order to identify causes and effects of the potential failure in design of the product, prioritize action plans to reduce the potential failures, track and evaluate results of the action plans and eventually minimize or eliminate the potential failure and the associated risk.

Typically, FMEAs are conducted manually, involving the use of excel spread sheets. This known technique proves to be time consuming and cumbersome in situations where the FMEA is being conducted for a product having a relatively large number of parts or numerous process steps. Additionally, the technique is prone to human errors. Moreover, in some instances, manually monitoring the progress of the FMEA, tracking the progress of the action plans or evaluating the success of risk mitigation may be difficult and challenging.

Design FMEA (DFMEA) done manually may leave some crucial part of circuitry unanalysed. The manual process does not ensure 100% coverage. Also a lot of reviews of the analysis report need to be performed. Therefore, there may a need for an automated system and method for performing the FMEA process and enabling an analyst to monitor and track the progress of risk mitigation. Much of the more recent document processing work has concentrated on distinguishing between mixed text and figures in documents, for example, optical character recognition of the text parts now being a reasonably standard operation. There has been some work done on interpreting engineering drawings but relatively little on processing electronic circuit diagrams.

The present invention is directed to overcoming one or more of the problems as set forth above.

SUMMARY OF THE INVENTION

Exemplary embodiments of the invention disclose method and system for automatically detecting tracks in electronic circuit schematics and highlighting them in a predefined colour.

According to an embodiment of the invention, a system and method for analysing electronic circuit schematics in an image format is disclosed. According to an exemplary embodiment, the disclosed system and method converts the electronic circuit schematic image into a binary image. A binary image matrix is constructed such that all the tracks and components are specified with a specific binary digit and the background is specified in other binary digit. The tracks are recreated isolating the components. The close loop tracks are identified and highlighted in a predefined colour in the image.

BRIEF DESCRIPTION OF DRAWINGS

Other objects, features, and advantages of the invention will be apparent from the following description when read with reference to the accompanying drawings. In the drawings, wherein like reference numerals denote corresponding parts throughout the several views:

Figure 1 illustrates a block diagram of a process for automatic track detection in electronic circuit schematics according to an exemplary embodiment of the invention.

Figure 2 illustrates an exemplary system identifying circuit track and for performing DFMEA analysis, according to one embodiment of the invention.

DETAILED DESCRIPTION OF DRAWINGS

The following description with reference to the accompanying drawings is provided to assist in a comprehensive understanding of exemplary embodiments of the invention as defined by the claims and their equivalents. It includes various specific details to assist in that

understanding but these are to be regarded as merely exemplary. Accordingly, those of ordinary skill in the art will recognize that various changes and modifications of the embodiments described herein can be made without departing from the scope and spirit of the invention. In addition, descriptions of well-known functions and constructions are omitted for clarity and conciseness.

According to embodiments of the invention, a system and method for tracing tracks in an electronic circuit diagram is disclosed wherein the diagram may be captured in PDF or image format.

FIG. 1 illustrates a block diagram of the process 100 for automatic track detection in electronic circuit schematic according to an embodiment of the invention. At step 102, an image of an electronic circuit schematic may be converted into a binary image. According to an embodiment, the image may correspond to a pdf format. According to yet another embodiment, the image may be in JPG, TIF, PNG, GIF or any other known image format. Using binary image, an image matrix may be constructed such that all tracks and components in the electronic circuit schematic are specified with a specific binary digit and background is specified in other binary digit. According to one embodiment of the invention, all the tracks and components may have a value of '0'in the image matrix and appear black and the background may have a value of '1' in the image matrix and appear white.

At step 104, the electronic circuit schematic image may be processed for automatically recreating tracks after isolating the components such as, but not limited to, ICs, resistors, capacitors, inductors etc. from the tracks.

At step 106, one or more close loop tracks may be identified from the recreated tracks. According to an embodiment, the closed loops may be highlighted in a predefined colour in the image to clearly differentiate the closed loop tracks from other tracks/components. According to yet another embodiment, the open loop tracks may be highlightcd in a predefined colour such that the colour used for open loop tracks is different from the colour used for closed loop tracks. A user may perform analysis by visually identifying the highlighted tracks.

FIG. 2 illustrates an exemplary system 200 for identifying circuit track in a circuit diagram and for performing DFMEA analysis, according to one embodiment of the present invention.

The disclosed system 200 may include an input module 202 for receiving an electronic circuit schematic in a predefined format. According to an embodiment, the circuit schematic may be in pdf format. The system 200 may have a processor 204 for scanning the entire electronic circuit schematic and for identifying all the tracks in the schematics on a one by one basis. The processor 204 may virtually isolate the components such as, but not limited to resistors, ICs, capacitors etc. from the track. The processor 204 may further highlight the tracks in the schematics one by one by converting them into a predefined colour. According to an embodiment, open and closed circuit tracks may be highlighted in different colours say blue and red respectively. According to further embodiment, the processor 204 may display highlighted tracks on a display device 206 such as but not limited to Cathode ray tube display (CRT), Light-emitting diode display (LED), Electroluminescent display (ELD), Plasma display panel (PDP) etc. to an analyst. According to one embodiment, the display may include a graphical user interface (GUI). The analyst may then have a choice whether to

analyse the highlighted track and any components in the highlighted track, or avoid the highlighted track.

The system 200 may allow the analyst to provide input for analysing thc track and the components involved. According to an embodiment, the system 200 may provide specific analysis fields according to a particular standard such as but not limited to MIL-1629A standards to the analyst. The analyst may select a specific track and review the highlighted tracks and may incorporate desirable changes in one or more analysis fields. The system 200 may enable placing of test points for analysis of track. According to yet another embodiment, the analyst may color the track after analysing the track. The colouring of the track may aid the analyst in keeping track of the coverage of the circuit schematic while performing DFMEA.

According to another embodiment, after analysis, the analyst may save the changes and the revised circuit schematic may be saved in a storage device 208.

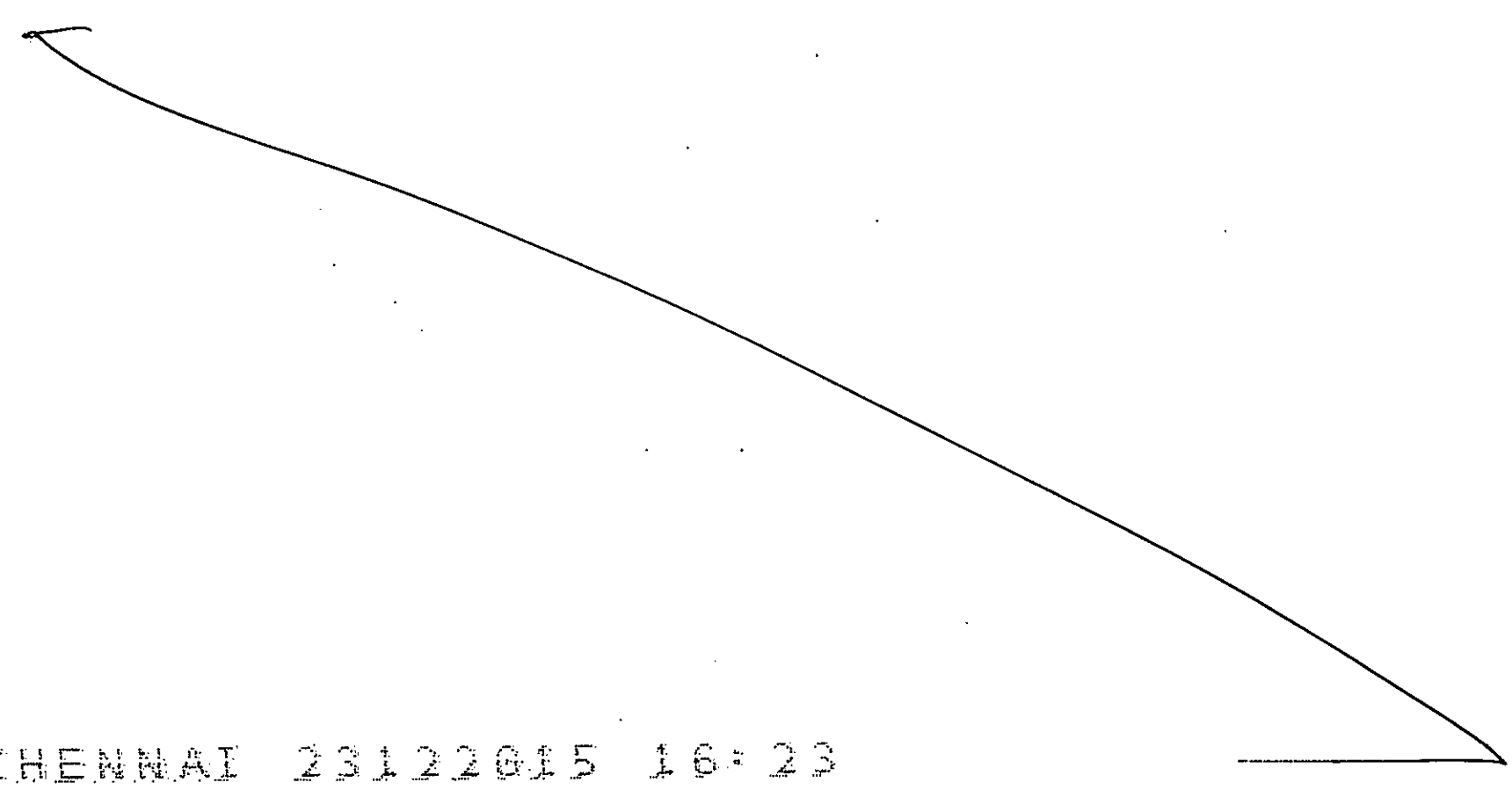
According to another embodiment of the invention, the system 200 may repeat the process for all the images in circuit schematic, in case the circuit schematic contains more than one image. According to yet another embodiment of the invention, the system 200 may generate a summary report after final circuit schematics is saved. Also, the system 200 may generate a new processed circuit schematic which shows highlighted tracks, components and test points on the tracks.

In the drawings and specification there has been set forth preferred embodiments of the invention, and although specific terms are employed, these are used in a generic and

descriptive sense only and not for purposes of limitation. Changes in the form and the proportion of parts, as well as in the substitution of equivalents, are contemplated as circumstances may suggest or render expedient without departing from the spirit or scope of the invention.

Throughout the various contexts described in this disclosure, the embodiments of the invention further encompass computer apparatus, computing systems and machine-readable media configured to carry out the foregoing systems and methods. In addition to an embodiment consisting of specifically designed integrated circuits or other electronics, the present invention may be conveniently implemented using a conventional general purpose or a specialized digital computer or microprocessor programmed according to the teachings of the present disclosure, as will be apparent to those skilled in the computer art.

Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will be apparent to those skilled in the software art. The invention may also be implemented by the preparation of application specific integrated circuits or by interconnecting an appropriate network of conventional component circuits, as will be readily apparent to those skilled in the art.



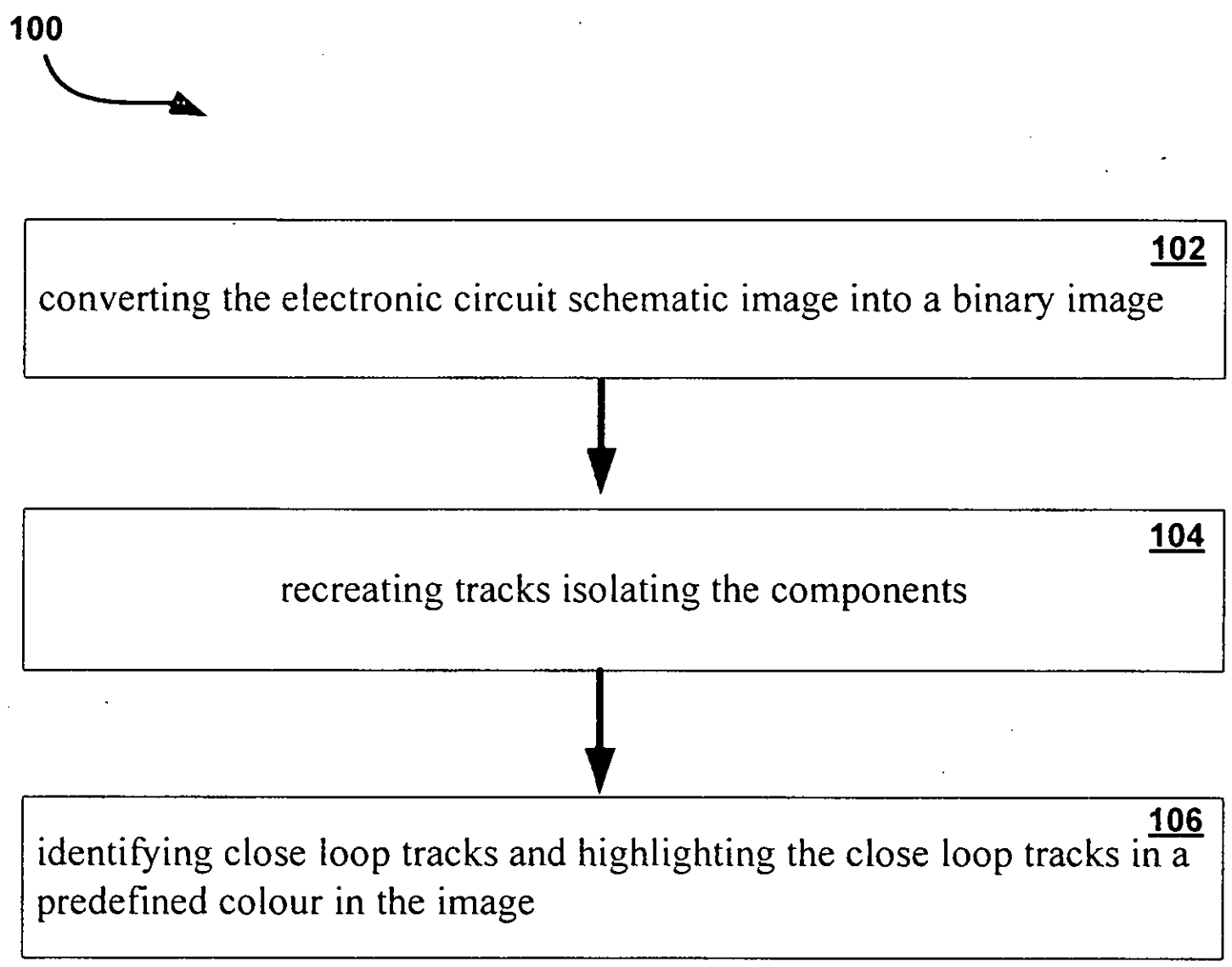


Figure 1

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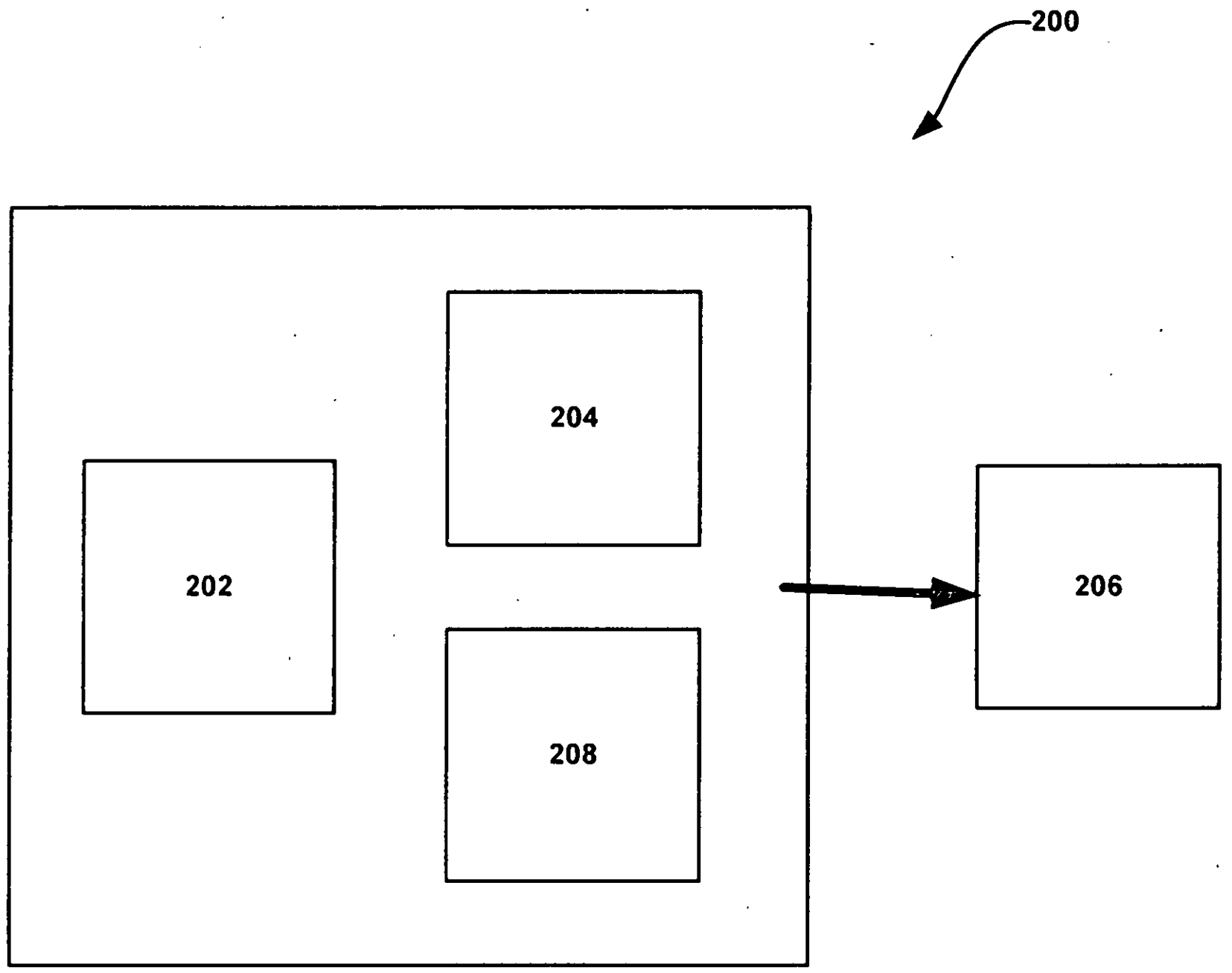

Figure 2

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