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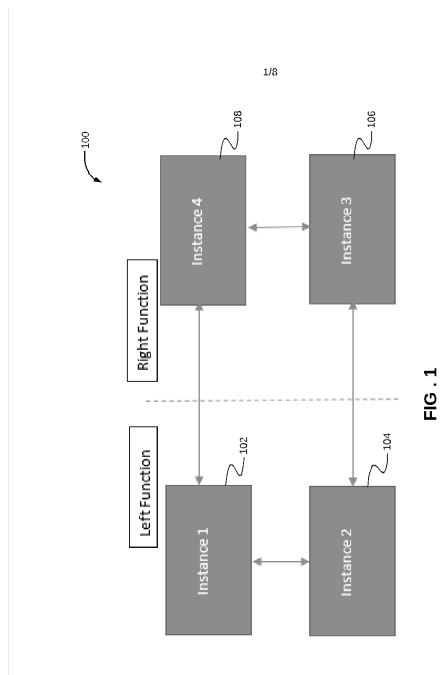
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(54) Title: METHOD AND SYSTEM TO EFFICIENTLY AND OPTIMALLY UTILIZE A HARDWARE CYCLIC REDUNDANCY CHECK (CRC) RESOURCE

(57) Abstract: In an embodiment, a method of optimally utilizing hardware Cyclic Redundancy Check (CRC) peripheral (206), in a dual redundant system is disclosed. The method may include transferring data from a first temporary buffer (204A) to a CRC peripheral (206), via a first DMA channel. The data from the first temporary buffer (204A) may be associated with a first instance (102). The method may further include upon completion of transfer of data from the first temporary buffer (204A) to the CRC peripheral (206), transferring data from a second temporary buffer (204B) to the CRC peripheral (206), via a second DMA channel. The data from the second temporary buffer (204B) may be associated with a second instance (104). The CRC peripheral (206) may be configured to perform CRC on the received data upon receiving the data from the first temporary buffer (204A) or the second temporary buffer (204B).



FORM 2

THE PATENTS ACT 1970
(39 OF 1970)
&
The Patent Rules, 2003
Complete Specification
(See Section 10 and Rule 13)

1. TITLE OF THE INVENTION

METHOD AND SYSTEM TO EFFICIENTLY AND OPTIMALLY UTILIZE A
HARDWARE CYCLIC REDUNDANCY CHECK (CRC) RESOURCE

2. APPLICANT(S)

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3. PREAMBLE TO THE DESCRIPTION

COMPLETE

The following specification particularly describes the invention and the manner in which
it is performed.

DESCRIPTION

Technical Field

[001] This disclosure relates generally to data integrity and validity, and more particularly to a method and a system for optimally and efficiently utilizing hardware Cyclic Redundancy Check (CRC) peripheral in a dual redundant system to deterministically validate data.

BACKGROUND

[002] In safety critical systems, redundancy, parallelism and synchronous working play important roles. When a system function is categorized as critical, such that failure of such system might lead to catastrophic outcomes, redundancy is introduced to reduce impact of failure. Typically, in redundant systems, active-passive relationship is used, in which one instance of system is active and another instance of system is passive, but is up-to-date and can switch over when active instance fails. When the system has multiple similar systems (instances) that have to work in synchronization, for example, engines on an aircraft, primary flight control system on wings of aircraft, etc., it is important that both the instances are synchronized and have data from opposite instance(s). Some systems employ both redundancy and synchronous working of instances. This results in two instances of function running on each channel, thereby making total number of instances four.

[003] Since each instance needs to be up-to-date with the data from other instances, data exchange and its validity between the instances plays an important role. Therefore, in a safety critical system, it is important that each instance computes the validity of data deterministically before consuming the data for taking decisions.

SUMMARY OF THE INVENTION

[004] In an embodiment, a method of optimally utilizing hardware Cyclic Redundancy Check (CRC) peripheral in a dual redundant system is disclosed. The method may include transferring

data from a first temporary buffer to a CRC peripheral, via a first DMA (Direct Memory Access) channel. The data from the first temporary buffer may be associated with a first instance. The method may further include upon completion of transfer of data from the first temporary buffer to the CRC peripheral, transferring data from a second temporary buffer to the CRC peripheral, via a second DMA channel. The data from the second temporary buffer may be associated with a second instance. The CRC peripheral may be configured to perform CRC on the received data upon receiving the data from the first temporary buffer or the second temporary buffer.

BRIEF DESCRIPTION OF THE DRAWINGS

10 [005] The accompanying drawings, which are incorporated in and constitute a part of this disclosure, illustrate exemplary embodiments and, together with the description, serve to explain the disclosed principles.

[006] FIG. 1 is a block diagram of a system employing different instances, in accordance with an embodiment of the present disclosure

15 [007] FIG. 2 is a block diagram of a system for optimally utilizing hardware Cyclic Redundancy Check (CRC) peripheral in a dual redundant system, in accordance with an embodiment of the present disclosure.

[008] FIG. 3 is a flowchart of a method of sequencing the incoming data through hardware Cyclic Redundancy Check (CRC) peripheral using DMA in a dual redundant system, in accordance with an embodiment of the present disclosure.

20 [009] FIGS. 4A-4E is a flowchart of a method of optimally utilizing hardware Cyclic Redundancy Check (CRC) peripheral in a dual redundant system, in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE DRAWINGS

[010] Exemplary embodiments are described with reference to the accompanying drawings. Wherever convenient, the same reference numbers are used throughout the drawings to refer to the same or like parts. While examples and features of disclosed principles are described herein, modifications, adaptations, and other implementations are possible without departing from the spirit and scope of the disclosed embodiments. It is intended that the following detailed description be considered as exemplary only, with the true scope and spirit being indicated by the following claims. Additional illustrative embodiments are listed below.

[011] Referring to FIG. 1, a block diagram of a system 100 employing different instances is illustrated, in accordance with an embodiment of the present disclosure. The system 100 may include four instances, for example, a first instance 102, a second instance 104, a third instance 106, and a fourth instance 108. For example, the system 100 may be an aircraft control system, and the four instances 102-108 may be dual redundant control systems within an aircraft. Further, the first instance 102 and the second instance 104 may correspond to the two instances (active-passive) controlling the left part of the aircraft, and the third instance 106 and the fourth instance 108 may correspond to the two instances (active-passive) controlling right part of the aircraft.

[012] It may be understood that these four instances have to work in synchronization. Therefore, it is important that the instances are synchronized and have data from opposite instance(s). As such, the system 100 may employ both redundancy and synchronous working of these instances, such that each instance needs to be up-to-date with the data from other instances. Further, redundancy is introduced to reduce impact of failure. An active-passive relationship is used, in which one instance of system is active and another instance of system is passive, but is up-to-date and can switch over when active instance fails. For example, the first instance 102 and the second instance 104 have active-passive relationship, and similarly the third instance 106 and the fourth instance 108 have active-passive relationship with each other.

[013] Data may be transmitted and received by each adjacent and opposite instance, for example, the first instance 102 may receive data from the fourth instance 108 and the second instance 104. This data received from both the fourth instance 108 and the second instance 104

has to be validated before it is consumed by the first instance 102. Similarly, the fourth instance 108 may receive data from the first instance 102 and the third instance 106. For example, the data may include sensor data, timing data, or any relevant data that may be needed for controlling the system 100. The data size and time to receive/transmit from each instance, may be determined
5 based on capability of interfacing elements of the system.

[014] Referring now to FIG. 2, a block diagram of a system 200 (corresponding to system 100) for optimally utilizing hardware Cyclic Redundancy Check (CRC) peripheral in a dual redundant system is illustrated, in accordance with an embodiment of the present disclosure. The system 200 may include a first peripheral buffer 202A and a second peripheral buffer 202B, a first
10 temporary buffer 204A and a second temporary buffer 204B, a CRC engine (also called CRC peripheral) 206, and a first application buffer 208A and a second application buffer 208B.

[015] By way of an example, the first peripheral buffer 202A and the second peripheral buffer 202B may receive data from an associated instance. For example, this data may be of 32 bits size. The first temporary buffer 204A and the second temporary buffer 204B may receive data
15 from the first peripheral buffer 202A and the second peripheral buffer 202B, respectively. For example, the data from the first peripheral buffer 202A may be associated with the second instance 104. Further, transfer of data from the first peripheral buffer 202A to the first temporary buffer 204A may be continued until predetermined amount of data is transferred. Further, it may be noted that the data from the second peripheral buffer 202B may be associated with the fourth
20 instance 108. Further, transfer of data from the second peripheral buffer 202B to the second temporary buffer 204B may be continued until predetermined amount of data is transferred.

[016] The data from the first temporary buffer 204A may be transferred to the CRC peripheral 206, via a DMA channel x2 (i.e. a first DMA channel). Upon completion of transfer of data from the first temporary buffer 204A to the CRC peripheral 206, the data from the second temporary
25 buffer 204B may be transferred to the CRC peripheral 206 via a DMA channel x5 (i.e. a second DMA channel). The CRC peripheral 206 may be configured to perform CRC on the received data upon receiving the data from the first temporary buffer 204A or the second temporary buffer 204B.

[017] Upon completion of transfer of data from the first temporary buffer 204A to the CRC peripheral 206, the transfer of data from the first temporary buffer 204A to the CRC peripheral 206 via the DMA channel x2 may be suspended. Further, the DMA channel x5 may be triggered to initiate transferring of data from the second temporary buffer 204B to the CRC peripheral 206.

5 Further, upon completion of transfer of data from the second temporary buffer 204B to the CRC peripheral 206, transfer of data from the second temporary buffer 204B to the CRC peripheral 206 via the DMA channel x5 may be suspended, and the DMA channel x2 may be triggered to initiate transferring of data from the first temporary buffer 204A to the CRC peripheral 206.

[018] It may be noted that upon performing of CRC by the CRC peripheral 206 on the data
10 received from the first temporary buffer 204A, this CRC data may be transferred to the first application buffer 208A. Further, upon performing of CRC by the CRC peripheral 206 on the data received from the second temporary buffer 204B, this CRC data may be transferred to the second application buffer 208B.

[019] Referring now to FIG.3, a flowchart 300 of a method of sequencing incoming data
15 through a hardware Cyclic Redundancy Check (CRC) peripheral using DMA in a dual redundant system is illustrated, in accordance with an embodiment of the present disclosure. It may be noted that DMA channels are configured independently with source, destination, and number of bytes to be transferred. The controlling point is triggering the DMA channels.

[020] In some embodiments, first, data may be received by and stored in a communication
20 peripheral buffer-1. The data stored in the communication peripheral buffer-1 may be transferred via a DMA channel-x1, and at the same time, data stored in a communication peripheral buffer-2 may be transferred via a DMA channel-x4. It may be noted that a microcontroller may include an interrupt which may trigger the DMA channels, once data is received in a communication peripheral buffer. Accordingly, once data is received in the communication peripheral buffer-1,
25 DMA channel-x1 may be triggered. Similarly, DMA channel-x4 may also be triggered nearly at the same time as the data may be coming at similar timelines from another instance. Once the data is received in the communication peripheral buffer-1, the data is transferred from the communication peripheral buffer-1 to a temporary buffer using the DMA channel-x1. Once that

is done, the DMA channel-x1 may trigger a DMA channel-x2 to transfer data from the temporary buffer into a CRC peripheral. Once the transfer of data from the temporary buffer into the CRC peripheral is complete, a DMA channel-x5 and a DMA channel-x3 may be triggered. The DMA channel-x3 may transfer the data to an application buffer-1, if CRC matches (as in stateflow).

5 Similarly, the DMA channel-x5 may transfer the data into the CRC peripheral. Once that is complete, a DMA channel-x6 may be triggered to transfer the data into an application buffer-2, and the sequence may be repeated.

[021] The stateflow may come in between to control the trigger for DMA channel-x5 and DMA channel-x2 which transfer the data into the CRC peripheral. It may be noted that during the time
10 period one of the DMA channel-x2 or DMA channel-x5 is transferring data into the CRC peripheral, the CRC peripheral may return a “BUSY” status. As a result, DMA channels cannot be triggered for data received on another communication peripheral buffer. The DMA channels may be triggered, only once the CRC peripheral return to a free state.

[022] In some embodiments, the computed CRC may be compared with a received CRC. If the
15 computed CRC does not match with the received CRC, a flag may be set to show CRC mismatch, so that the application does not use the data in application buffer.

[023] The method 300 is further represented in a step-by-step form via FIGS. 4A-4E. As shown
in FIGS. 4A-4E, a flowchart of a method 400 of optimally utilizing hardware Cyclic Redundancy Check (CRC) peripheral in a dual redundant system is illustrated, in accordance with an
20 embodiment of the present disclosure.

[024] The present disclosure discusses various techniques for optimizing hardware CRC peripheral use in a dual redundant system. The techniques employ DMA channels for data transfer. Further, the techniques provide for switching between buffers and selective triggering of DMAs for optimal use of CRC peripheral with multiple instances, avoiding loss of any data,
25 and avoiding a race condition between different instances. In other words, a situation is avoided where two DMA channels are trying to access the CRC peripheral. Further, the techniques provide for efficient data utilization, as the data is not straightaway transferred to the to the application, but is first stored and accumulated in a temporary buffer. The CRC is computed, and

when the CRC is determined to be acceptable, a flag is updated to show valid data. If CRC is not acceptable, then final buffer is updated with data, and a flag is updated to show invalid data.

[025] The techniques provide a unique solution of optimally utilizing the hardware resource used for computing CRC for a dual redundant system, thereby reducing load on software. For example, the techniques provide for using a single CRC peripheral for computing the CRC of received data from multiple instances. Further, software is used for configuring DMA and CRC peripherals, triggering the DMA channels for data transfers and logic to avoid raise conditions, and re-triggering the DMA channels in situation error is returned by a DMA channel. Moreover, the techniques provide for efficient coding in terms of smaller code footprint and lower execution timing, thereby reducing the cost of controller and overall product price.

[026] It is intended that the disclosure and examples be considered as exemplary only, with a true scope and spirit of disclosed embodiments being indicated by the following claims.

CLAIMS

We Claim:

1. A method of optimizing Cyclic Redundancy Check (CRC) in a dual redundant system, the method comprising:

5 transferring, by a processing device, data from a first temporary buffer (204A) to a CRC peripheral (206), via a first DMA channel, wherein the data from the first temporary buffer (204A) is associated with a first instance (102) (102); and

 upon completion of transfer of data from the first temporary buffer (204A) to the CRC peripheral (206), transferring, by the processing device, data from a second temporary buffer (204B) to the CRC peripheral (206), via a second DMA channel, wherein the data from the
10 second temporary buffer (204B) is associated with a second instance (104), and wherein the CRC peripheral (206) is configured to perform CRC on the received data upon receiving the data from the first temporary buffer (204A) or the second temporary buffer (204B) .

15 **2.** The method as claimed in claim 1, further comprising:

 transferring data from a first peripheral buffer (202A) to the first temporary buffer (204A), wherein the data from the first peripheral buffer (202A) is associated with the first instance (102), and wherein transfer of data from the first peripheral buffer (202A) to the first temporary buffer (204A) is continued until predetermined amount of data is
20 transferred; and

 transferring data from a second peripheral buffer (202B) to the second temporary buffer (204B), wherein the data from the second peripheral buffer (202B) is associated with the second instance, and wherein transfer of data from the second peripheral buffer (202B) to the second temporary buffer (204B) is continued until predetermined amount of data is
25 transferred.

3. The method as claimed in claim 1, further comprising:

 upon completion of transfer of data from the first temporary buffer (204A) to the CRC peripheral (206),

suspending transfer of data from the first temporary buffer (204A) to the CRC peripheral via the first DMA channel; and

triggering the second DMA channel to initiate transferring of data from the second temporary buffer (204B) to the CRC peripheral (206).

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4. The method as claimed in claim 3, further comprising:

upon completion of transfer of data from the second temporary buffer (204B) to the CRC peripheral (206),

10 suspending transfer of data from the second temporary buffer (204B) to the CRC peripheral (206) via the second DMA channel; and

triggering the first DMA channel to initiate transferring of data from the first temporary buffer (204A) to the CRC peripheral (206).

5. The method as claimed in claim 1, further comprising:

15 upon performing of CRC by the CRC peripheral (206) on the data received from the first temporary buffer (204A), transferring the CRC data to a first application buffer (208A); and

20 upon performing of CRC by the CRC peripheral (206) on the data received from the second temporary buffer (204B), transferring the CRC data to a second application buffer (208B).

Dated this 30th day of June 2020

25

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ABSTRACT

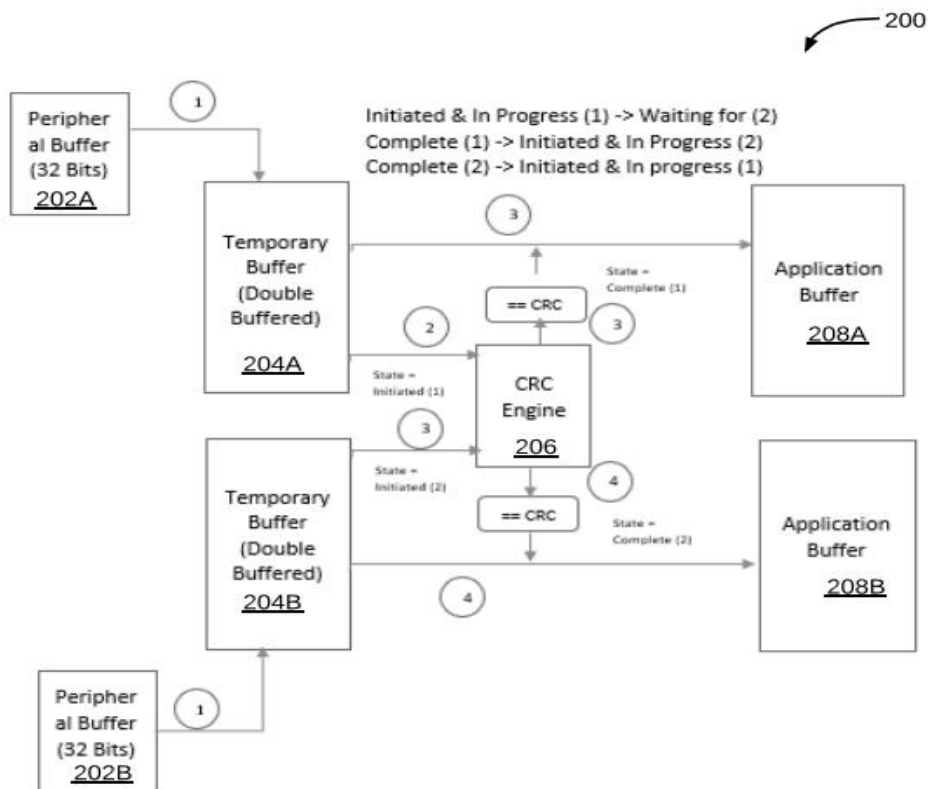
METHOD AND SYSTEM TO EFFICIENTLY AND OPTIMALLY UTILIZE A HARDWARE CYCLIC REDUNDANCY CHECK (CRC) RESOURCE

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In an embodiment, a method of optimally utilizing hardware Cyclic Redundancy Check (CRC) peripheral (206), in a dual redundant system is disclosed. The method may include transferring data from a first temporary buffer (204A) to a CRC peripheral (206), via a first DMA channel. The data from the first temporary buffer (204A) may be associated with a first instance (102). The method may further include upon completion of transfer of data from the first temporary buffer (204A) to the CRC peripheral (206), transferring data from a second temporary buffer (204B) to the CRC peripheral (206), via a second DMA channel. The data from the second temporary buffer (204B) may be associated with a second instance (104). The CRC peripheral (206) may be configured to perform CRC on the received data upon receiving the data from the first temporary buffer (204A) or the second temporary buffer (204B).

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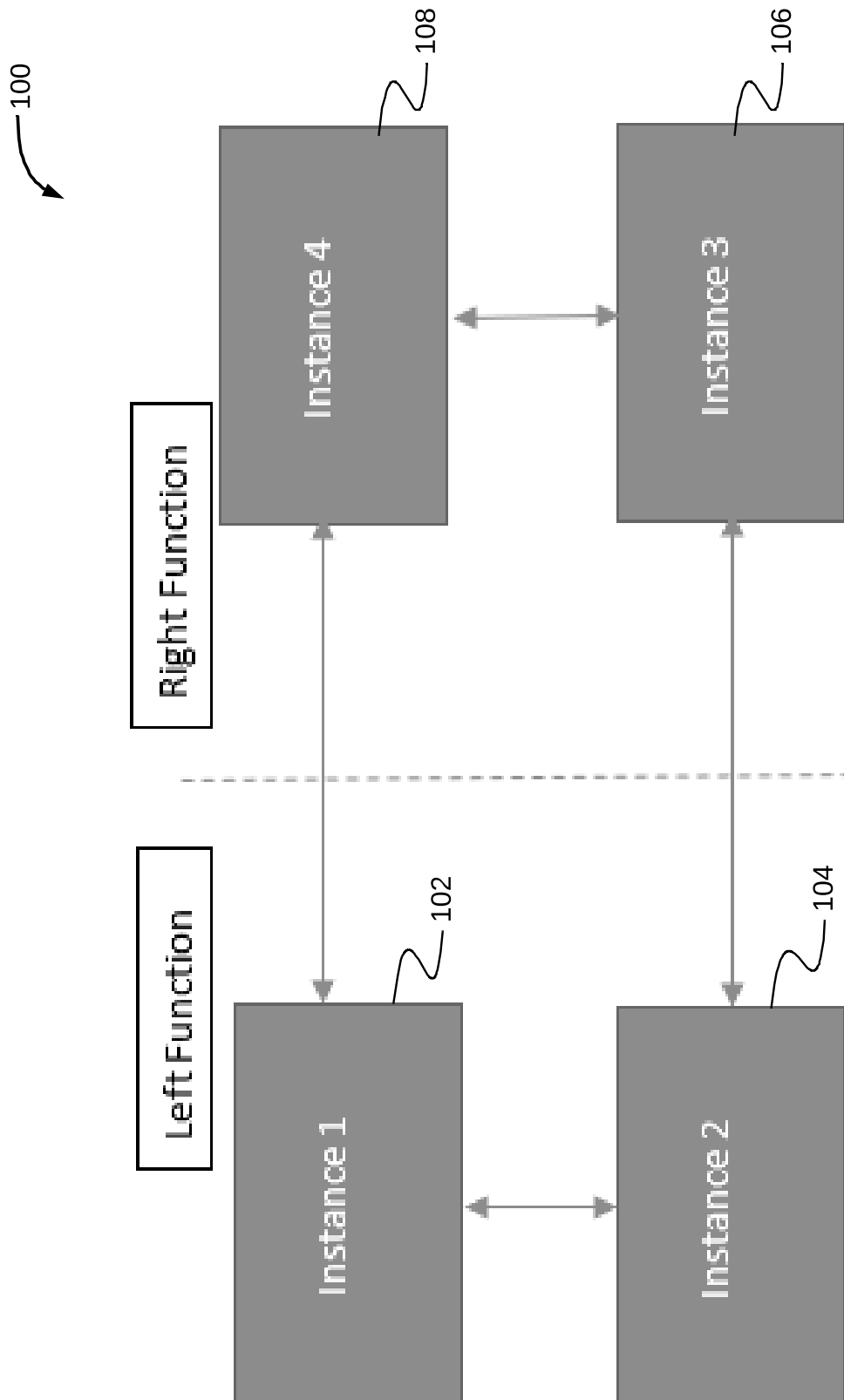


FIG . 1

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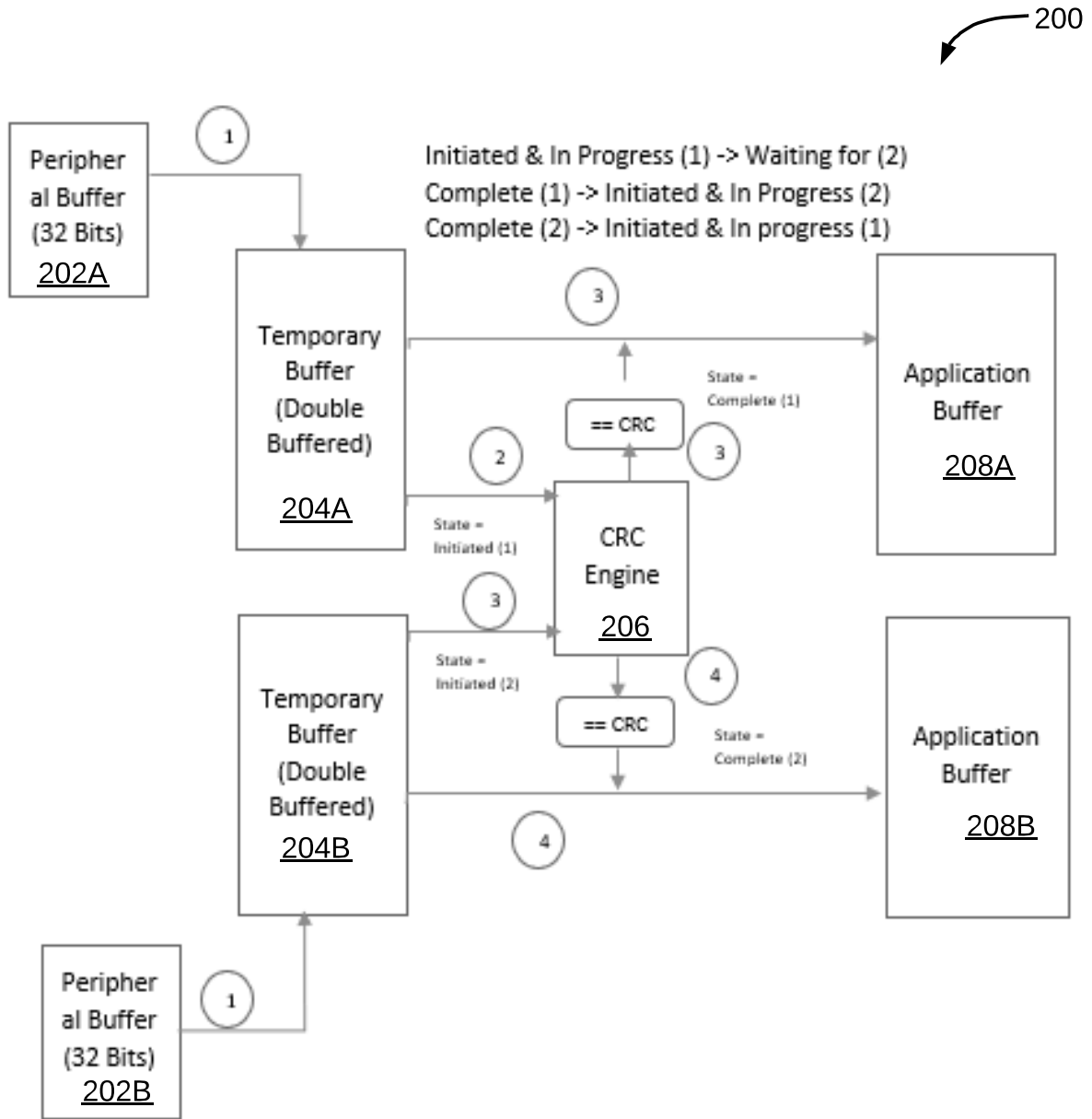


FIG . 2

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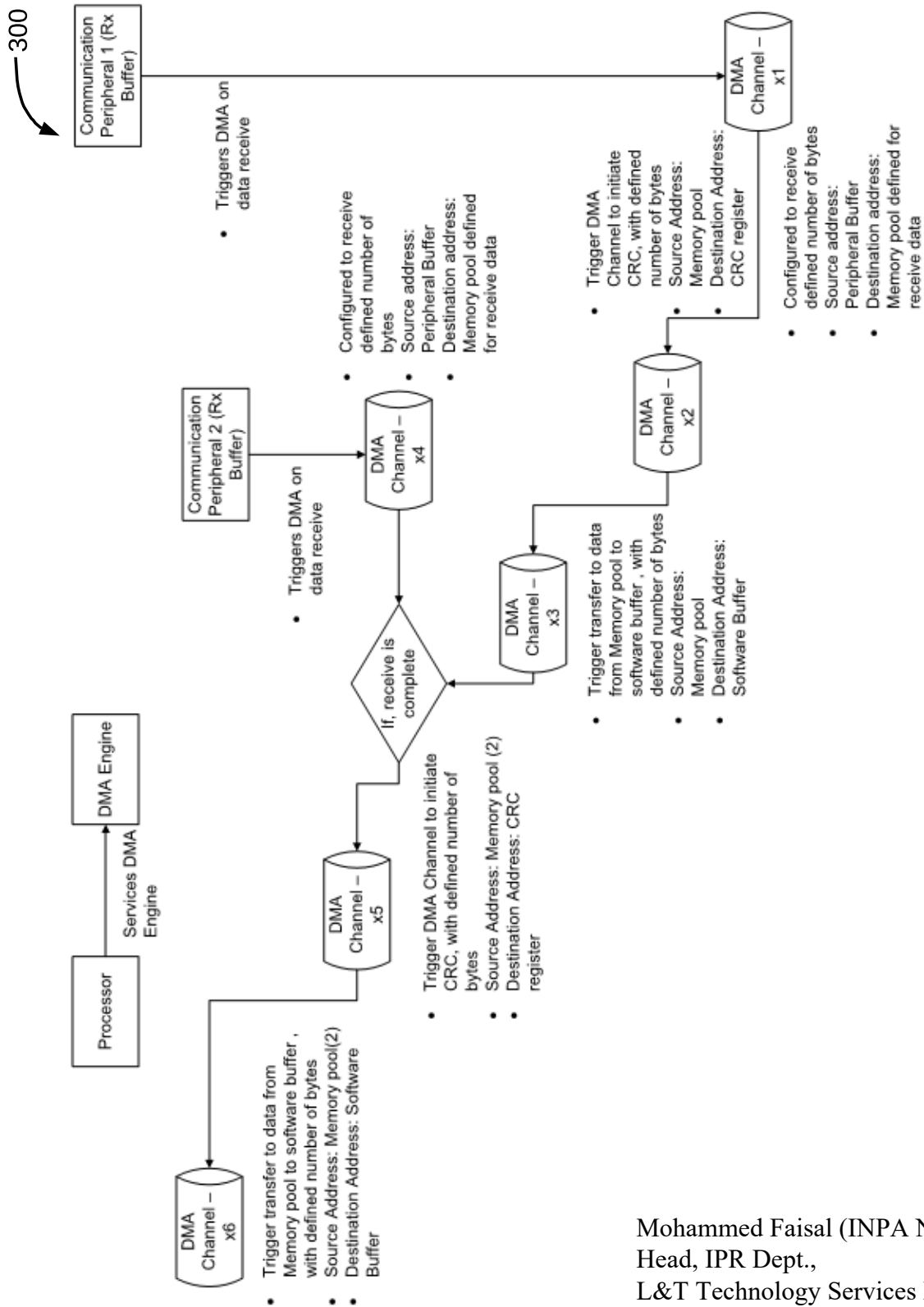


FIG . 3

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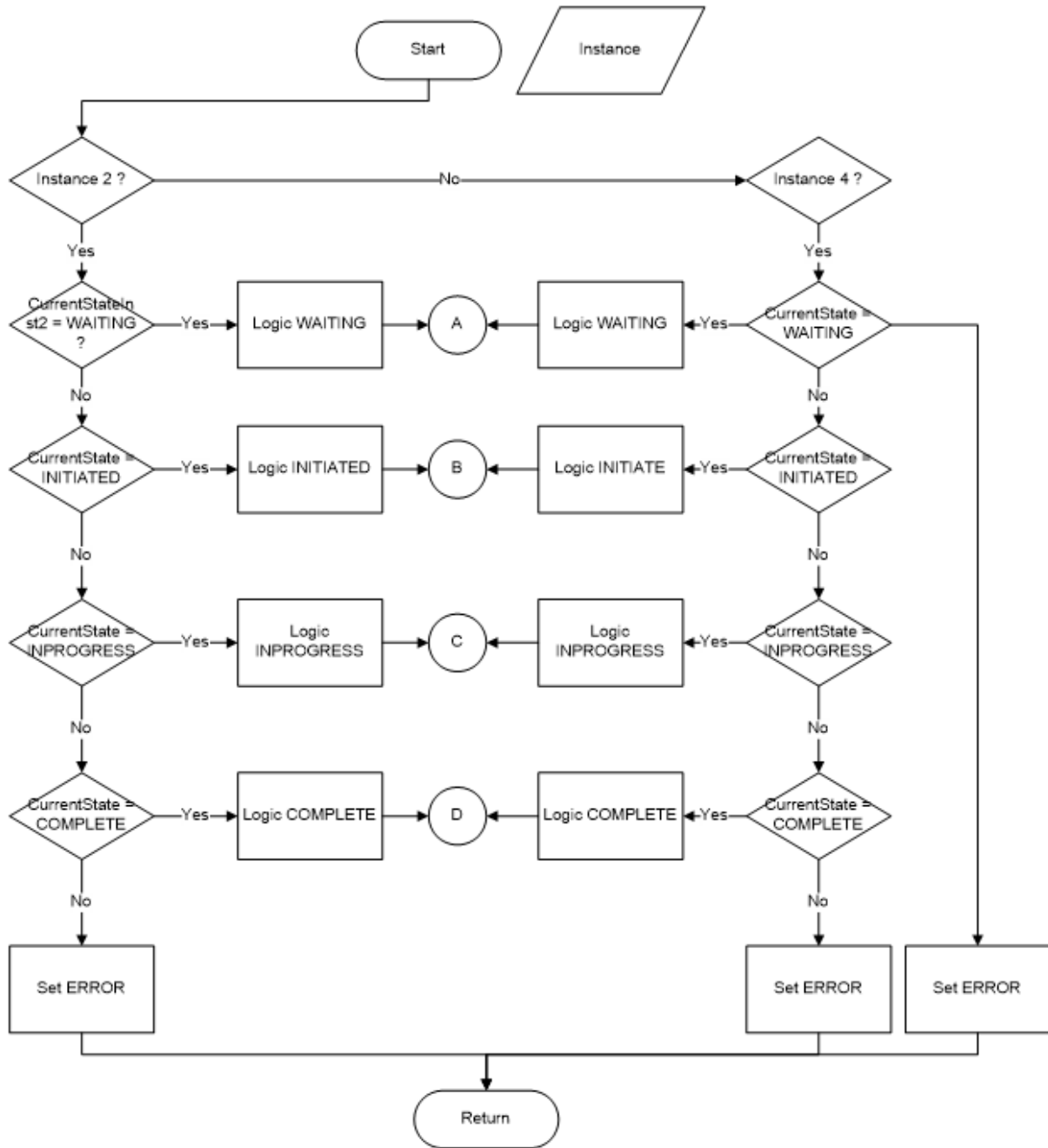


FIG . 4A

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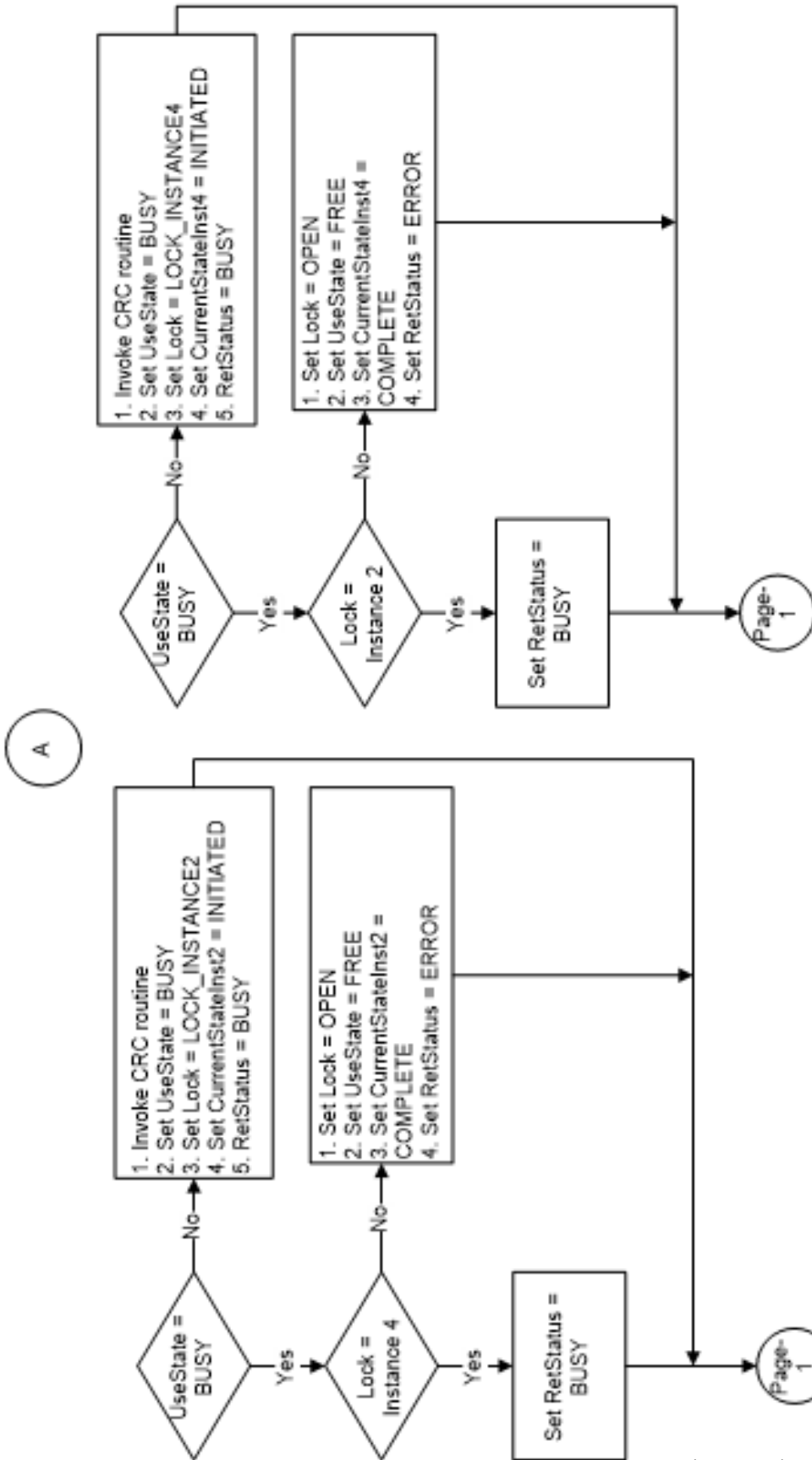


FIG . 4B

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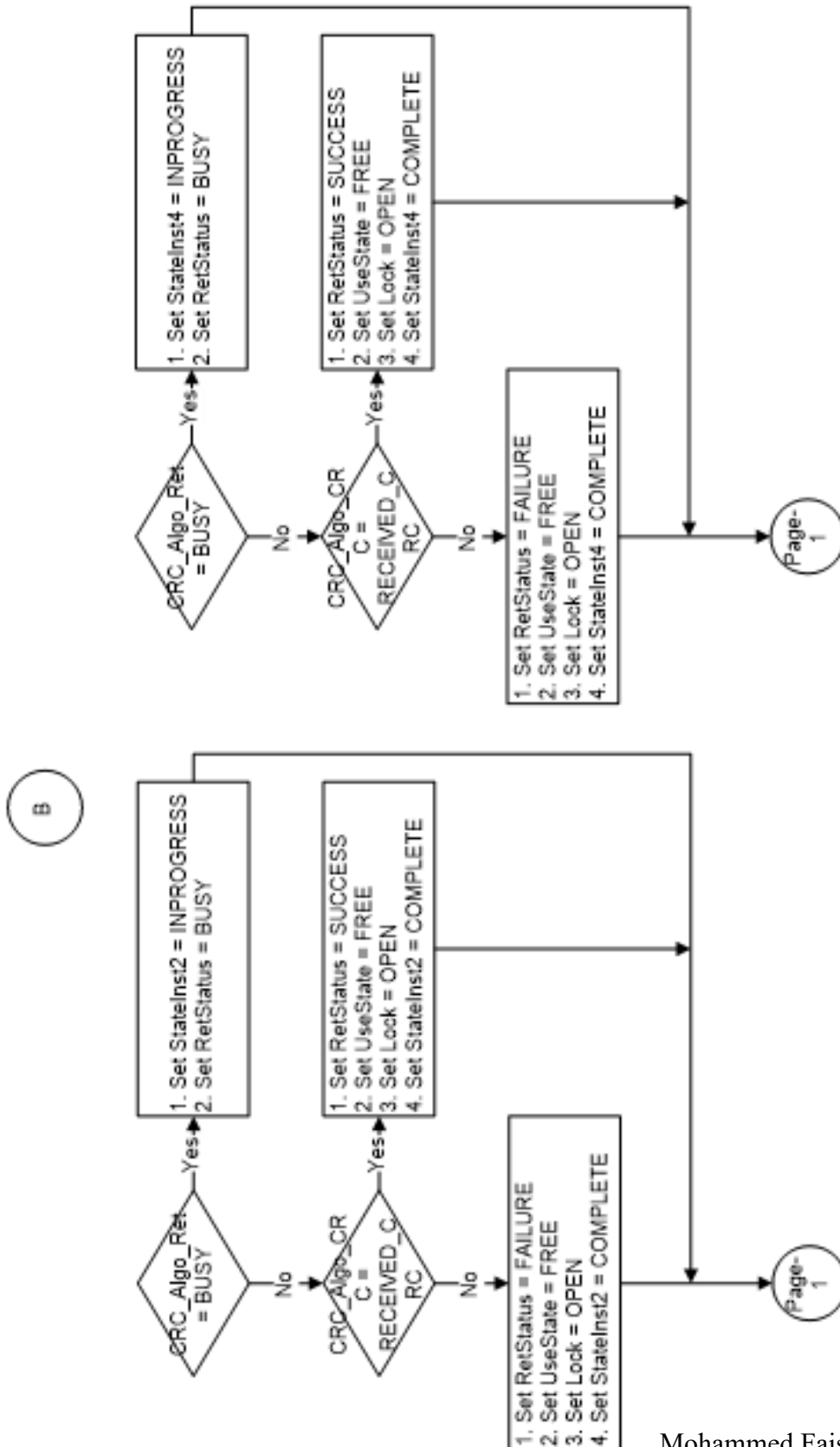


FIG . 4C

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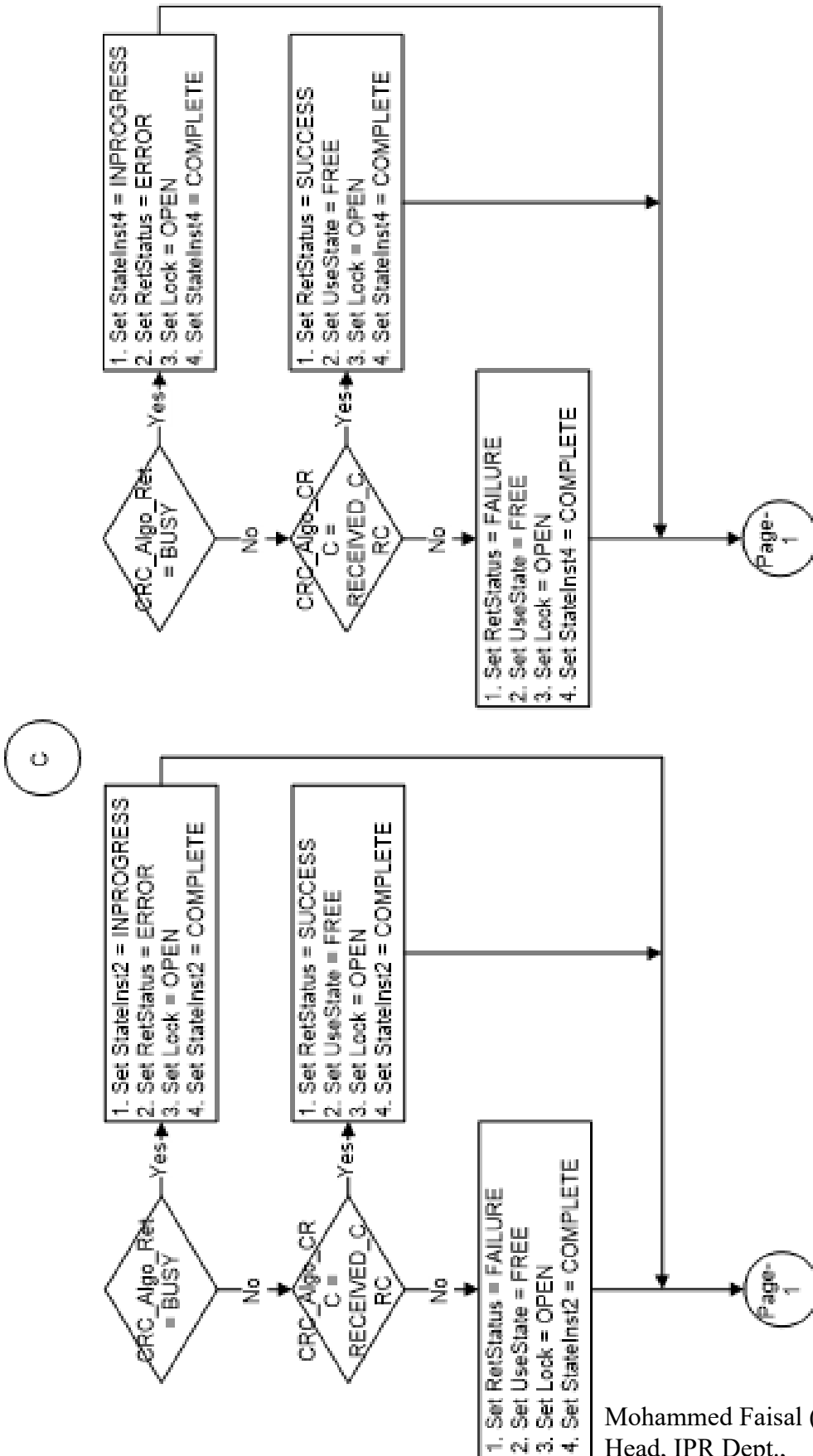


FIG. 4D

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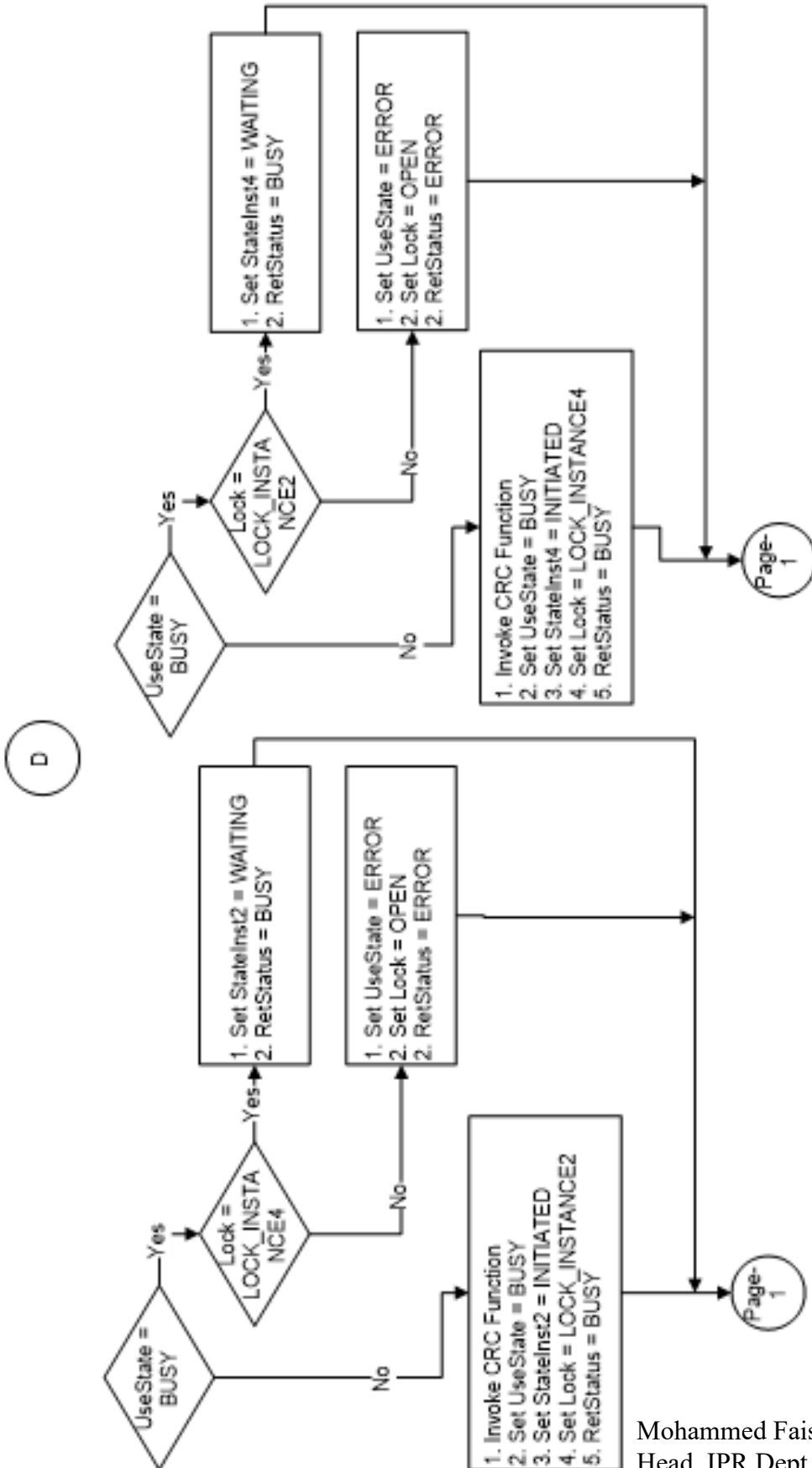


FIG. 4E

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