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(54) Title: SYSTEM AND METHOD FOR TESTING DEVICES

(57) Abstract: The present invention relates a system and method for testing plurality of devices. The method recites providing one or more signals to operate a plurality of control units of a simulation model, on the basis of the type of DUT, to allow the simulation model to generate plurality of test signals. The method recites simulating a test environment for the DUT using the test signals. The method further comprises configuring a plurality of I/O ports based on the simulated test environment. Further, the method comprises transmitting the generated test signals to the DUT via a plurality of communication channels and receiving feedback signals from the DUT, via the plurality of communication channels, in response to transmitting the plurality of test signals. Furthermore, the method comprises processing the feedback signals and generating a test report and sharing the generated test report with a host computing device.

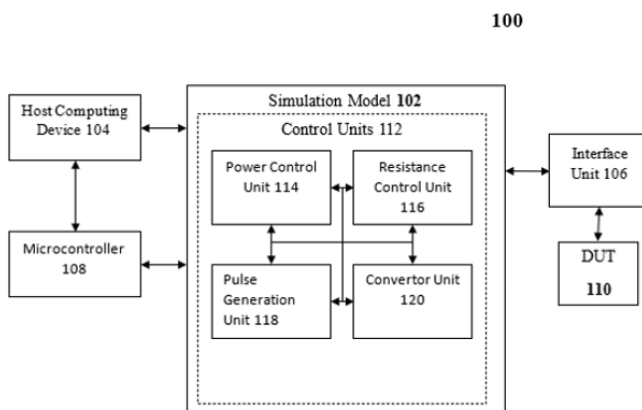


Fig. 1

FORM 2

THE PATENTS ACT 1970
(39 OF 1970)

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The Patent Rules, 2003

Complete Specification

(See Section 10 and Rule 13)

1. TITLE OF THE INVENTION

SYSTEM AND METHOD FOR TESTING DEVICES

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3. PREAMBLE TO THE DESCRIPTION

COMPLETE

The following specification describes the invention and the manner in which it is to be performed

DESCRIPTION

TECHNICAL FIELD

5 [0001] The present subject matter described herein, in general, discloses system and method for testing a plurality of devices. Particularly, the present disclosure relates to a low cost and less complex automotive hardware in loop testing system.

BACKGROUND OF THE INVENTION

10 [0002] Hardware-in-the-loop (HIL) simulation-based testing of the Electronic Control Modules (ECMs) is widespread. A testing system typically includes a Hardware-in-the-loop (HIL) system, a host system, and the ECM that to be tested. The HIL system includes a simulation model of a machine and/or an engine system of the machine. The simulation model is a user programmable environment. The host system is used to communicate with a user while providing inputs to the HIL system and receiving output from the HIL system as well as from
15 the ECM.

[0003] The simulation model in the HIL system is programmable using a desktop automation application on the host system. The desktop automation application is also configured to send, receive and analyse the output from the ECM and HIL system. A
20 communication channel, such as Controller Area Network (CAN), is used to send ECM output signals to the host system which can be monitored and compared with the output from the HIL system. However, conventional HIL system require assembling of numerous hardware entities together to test a plurality of devices. Moreover, assembling numerous hardware entities together at one place for desired testing of automotive units is more complex and more costly.

25 [0004] Thus, there is need of techniques which are more cost effective and simpler ways for testing a device.

SUMMARY OF THE INVENTION

[0005] The present disclosure overcomes one or more shortcomings of the prior art and provides additional advantages discussed throughout the present disclosure. Additional features and advantages are realized through the techniques of the present disclosure. Other embodiments and aspects of the disclosure are described in detail herein and are considered a part of the claimed disclosure.

[0006] In one non-limiting embodiment of the present disclosure, a system for testing a plurality of devices is proposed. The system comprises a simulation model configured to simulate a test environment for a device under test (DUT) using a plurality of test signals. Said simulation model comprises a plurality of control units configured to generate the plurality of test signals based on the type of DUT. The system further comprises a host computing device operatively coupled to the simulation model. The host computing device is configured to provide one or more signals to operate the plurality of control units, on the basis of the type of DUT, so as to allow the simulation model to generate the plurality of test signals and configure a plurality of input/output (I/O) ports based on the simulated test environment. The system furthermore comprises an interface unit comprising the plurality of I/O ports. Said I/O ports being configured to: transmit the plurality of generated test signals to the DUT via a plurality of communication channels and receive one or more feedback signals from the DUT, via the plurality of communication channels, in response to transmitting the plurality of test signals. The system furthermore comprises a microcontroller operatively coupled with the simulation model. Said microcontroller is configured to: process the one or more feedback signals and generate a test report and share the generated test report with the host computing device.

[0007] In another non-limiting embodiment of the present disclosure the plurality of control units comprise a power control unit to generate controlled power signals for testing the DUT, a resistance controlling unit to generate resistive signals for testing the DUT, a pulse generation unit to generate modulated pulse signals for testing the DUT, and a convertor unit comprising an analog to digital (ADC) converter to convert analog signals into digital signals and a digital to analog (DAC) converter to convert digital signals into analog signals.

[0008] In yet another non-limiting embodiment of the present the host computing device is further configured to adjust the one or more signals provided to the plurality of control units to

control their operations, in response to the one or more feedback signals received by the simulation model.

5 [0009] In yet another non-limiting embodiment of the present disclosure, the host computing device further comprises: a processing unit configured to analyse the received test report, and a display unit configured to display the test results based on the test report.

10 [0010] In yet another non-limiting embodiment of the present disclosure, the simulation model is configured to communicate with the host computing unit via a serial communication port.

[0011] In yet another non-limiting embodiment of the present disclosure, the host computing unit comprises plurality of APIs configured to: control the operations of plurality of I/O ports, and regulate the one or more signals to the plurality of control units.

15 [0012] In yet another non-limiting embodiment of the present disclosure, the simulation model further comprises: a plurality of switches, a power switching unit, and a relay control unit.

20 [0013] In yet another non-limiting embodiment of the present disclosure, a method for testing a device is disclosed. The method comprises providing one or more signals to operate a plurality of control units of a simulation model, on the basis of the type of a device under test (DUT), so as to allow the simulation model to generate a plurality of test signals. The method further comprises simulating a test environment for the DUT using the plurality of test signals.

25 The method further comprises configuring a plurality of input/output (I/O) ports based on the simulated test environment. Further, the method recites transmitting the plurality of generated test signals to the DUT via a plurality of communication channels. The method furthermore comprises receiving one or more feedback signals from the DUT, via the plurality of communication channels, in response to transmitting the plurality of test signals, processing

30 the one or more feedback signals and generating a test report. Lastly, the method comprises sharing the generated test report with a host computing device.

[0014] In yet another non-limiting embodiment of the present disclosure, the method further comprises adjusting the one or more signals provided to the plurality of control units to control

their operations, in response to the one or more feedback signals received by the simulation model.

5 [0015] In yet another non-limiting embodiment of the present disclosure, the method further comprises analysing the test report and displaying the test results based on the test report.

OBJECTIVES OF THE INVENTION

10 [0016] An objective of the present invention is to provide a system and a method for testing a plurality of device which is less complex and can perform testing in cost-effective and efficient manner.

[0017] Another objective of the present invention is to provide a Bench Level Test Setup for testing the devices.

15 [0018] Yet another objective of the present invention is to provide a scalable architecture for testing the plurality of devices.

[0019] Yet another objective of the present invention is to provide a system for early testing at developer level.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The accompanying drawings, which are incorporated in and constitute a part of this disclosure, illustrate exemplary embodiments and, together with the description, serve to explain the disclosed embodiments. In the figures, the left-most digit(s) of a reference number identifies the figure in which the reference number first appears. The same numbers are used throughout the figures to reference like features and components. Some embodiments of system and/or methods in accordance with embodiments of the present subject matter are now described, by way of example only, and with reference to the accompanying figures, in which:

30 [0021] Fig. 1 illustrates a block diagram of a system for testing a plurality of devices, in accordance with an embodiment of the present subject matter.

[0022] Fig. 2 illustrates an exemplary setup of the system for testing the plurality of devices, in accordance with an embodiment of the present subject matter.

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[0023] Fig. 3 is a flow diagram illustrating a method for testing a plurality of devices, in accordance with an embodiment of the present subject matter.

5 [0024] Fig. 4 illustrates an exemplary structure of various units of the system, in accordance with an embodiment of the present subject matter.

[0025] Fig. 5 illustrates an exemplary structure of various units of the system, in accordance with an embodiment of the present subject matter.

10 [0026] It should be appreciated by those skilled in the art that any block diagrams herein represent conceptual views of illustrative systems embodying the principles of the present subject matter. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudo code, and the like represent various processes which may be substantially represented in computer readable medium and executed by a computer or
15 processor, whether or not such computer or processor is explicitly shown.

DETAILED DESCRIPTION

[0027] In the present document, the word “exemplary” is used herein to mean “serving as an
20 example, instance, or illustration.” Any embodiment or implementation of the present subject-matter described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments.

[0028] While the disclosure is susceptible to various modifications and alternative forms,
25 specific embodiment thereof has been shown by way of example in the drawings and will be described in detail below. It should be understood, however that it is not intended to limit the disclosure to the particular forms disclosed, but on the contrary, the disclosure is to cover all modifications, equivalents, and alternatives falling within the scope of the disclosure.

30 [0029] The terms “comprises”, “comprising”, “include(s)”, or any other variations thereof, are intended to cover a non-exclusive inclusion, such that a setup, system or method that comprises a list of components or steps does not include only those components or steps but may include other components or steps not expressly listed or inherent to such setup or system or method. In other words, one or more elements in a system or apparatus proceeded by

“comprises... a” does not, without more constraints, preclude the existence of other elements or additional elements in the system or apparatus.

5 [0030] In the following detailed description of the embodiments of the disclosure, reference is made to the accompanying drawings that form a part hereof, and are shown by way of illustration of specific embodiments in which the disclosure may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the disclosure, and it is to be understood that other embodiments may be utilized and that changes may be made without departing from the scope of the present disclosure. The following
10 description is, therefore, not to be taken in a limiting sense.

[0031] The present invention will be described herein below with reference to the accompanying drawings. In the following description, well known functions or constructions are not described in detail since they would obscure the description with unnecessary detail.

15 [0032] The present disclosure recites a system for performing testing of a plurality of devices. The system uses I/O ports suitable for any automotive ECU for black box /functional testing at low cost. Also, the system comprises customizable drivers and APIs that can be integrated with Python. The system also comprises easily scalable test hardware and test software platform.

20 [0033] Referring to figure 1, a system 100 for testing a plurality of devices. The system 100 comprises a simulation model 102, a host computing device 104, an interface unit 106, a microcontroller 108 operatively coupled to each other to test a device which is under test (DUT) 110. According to an embodiment of the present disclosure, the simulation model 102, the host
25 computing device 104, the interface unit 106, and the microcontroller 108 are communicatively coupled with each other via a wired or wireless link.

[0034] According to an exemplary embodiment, the simulation model 102 communicates with the host computing device 104 via a serial communication port, but not limited thereto.
30 Further, the simulation model 102 comprises a plurality of control units 112 which provide various signals to test the DUT 110. For example, the simulation model 102 comprises a power control unit 114 to generate controlled power signals for testing the DUT 110, a resistance controlling unit 116 to generate resistive signals for testing the DUT 110, a pulse generation unit 118 to generate modulated pulse signals for testing the DUT 110, and a convertor unit 120
35 comprising an analog to digital (ADC) converter to convert analog signals into digital signals

and a digital to analog (DAC) converter to convert digital signals into analog signals. Those skilled in the art will appreciate that the control units 112 shown in figure 1 disclose one exemplary embodiment required for the implementing the invention. However, the design of the control units 112 is reconfigurable as per the need, specifically based on the requirement of the DUT 110. An exemplary setup of the system 100 is shown in fig. 2, which is explained below with reference to an exemplary application of the system.

[0035] The simulation model 102 is configured to simulate a test environment for the DUT 110 using the plurality of test signals which are generated by the plurality of control units 112. In an exemplary aspect, the control unit 112 are configured to generate these test signals based on the type of the DUT 110. Further, it may be noted that the plurality of control units 112 are operated based on one or more signals provided by the host computing device 104. Thus, it may be appreciated that the host computing device 104 provides the one or more signals to operate the plurality of control units 112, on the basis of the type of DUT 110, so as to allow the simulation model 102 to generate the plurality of test signals. Further, in another exemplary aspect, the host computing device 104 is also configured to manage a plurality of input/output (I/O) ports, of the interface unit 106, based on the simulated test environment. Those skilled in the art will appreciate that, based on the requirement, said system 100 may be re-align the I/O ports of the interface unit 106.

[0036] As discussed above, the interface unit 106 may comprise the plurality of I/O ports and said I/O ports may be configured to transmit the plurality of generated test signals to the DUT 110 via a plurality of communication channels. Further, the I/O ports may be also configured to receive one or more feedback signals from the DUT 110, via the plurality of communication channels, in response to transmitting the plurality of test signals.

[0037] Moving ahead, as shown in figure 1, the microcontroller 108 connected to the simulation model 102 and the host computing device 104 may be configured to receive the one or more feedback signals from the DUT 110. The microcontroller 108 is further configured to process the one or more feedback signals and generates a test report for the DUT 110. The microcontroller 108 is then configured to share the generated test report with the host computing device 104. The host computing device 104 further comprises a processing unit and a display unit. The processing unit analyses the received test report, and the display unit displays the test results based on the test report. According to an embodiment of the present disclosure, analysing the received test report may comprise generating test results in form of a

short summary or key information of the test report by analysing the test report. Such test results may be helpful to review the testing of the DUT in an effective manner.

5 **[0038]** According to an embodiment, the host computing device 104 may also be configured adjust the one or more signals provided to the plurality of control units 112 to control their operations, in response to the one or more feedback signals received by the simulation model 102. Further, the host computing device 104 also comprises plurality of APIs to control the operations of plurality of I/O ports and regulate the one or more signals to the plurality of control units 112.

10 **[0039]** The operation of the system 100 may be easily understood by way of following example being implemented by means of fig. 2. The system of fig. 2 may be used for Inverter testing (inside hybrid vehicle) for faulty cooling system when driving. Thus, the DUT in fig. 2 may be an inverter unit which is to be tested.

15 **[0040]** The micro-HIL (μ HIL) box in fig. 2 represents the simulation model 102 of the system which is configured to generate a simulation environment for testing the inverter unit (DUT 110). Particularly, the μ HIL102 may simulate an environment for a motor (not shown) inside a hybrid vehicle controlled by an Inverter (DUT) and the inverter can take care of the motor control when the torque currents are high, and cooling is either low or not working to safely turn off motor when the temperature goes above maximum limit.

20 **[0041]** The hosting PC represents the host computing device 104, which may provide signal to the μ HIL to generate the speed and torque command signals. The GPIOs of fig. 2 represents the I/O ports of interface unit 108 of the system 100, which may be configured to communicate the speed and torque command signals to inverter under test, via the communication channel such as CAN. In an embodiment, the PWMs represents the Pulse generation unit 118 of the system 100. The PWMs may generate speed signals to simulate the environment required for testing inverter. Similarly, the torque signals may be simulated using internal variable. The
30 selectable resistor represents the resistance control unit 116 of the system 100. The motor temperature can be set to nominal using the selectable resistor to simulate the nominal as well as high temperature. The response or fault from DUT may be verified using the feedback signal such as CAN message from DUT. In this manner, automation of above actions can be done using the system drivers (Firmware) and API to trigger the driver functions.

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[0042] In this manner, the system illustrated in fig. 2 may test the plurality of devices in an effective manner and at low cost because the system comprises combination of various control units which may generate various test signals suitable for testing the plurality of device.

5 [0043] Fig. 3 discloses a method 300 for testing a plurality of devices. At step 302, the method 300 comprises providing one or more signals, from the host computing device 104, to operate a plurality of control units 112 of the simulation model 102, to allow the simulation model 102 to generate a plurality of test signals. The signals are provided on the basis of the type of the DUT 110.

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[0044] At step 304, the method 300 recites simulating a test environment for the DUT 110 using the plurality of test signals. At step 306, the method 300 recites configuring the plurality of I/O ports based on the simulated test environment, by the host computing device 104. Further, at step 308, the method 300 recites transmitting the plurality of generated test signals to the DUT 110 via a plurality of communication channels.

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[0045] The method 300 at step 310 recites receiving one or more feedback signals from the DUT 110, via the plurality of communication channels, in response to transmitting the plurality of test signals. The DUT 110 may generate feedback signals based on the received test signals. Further, at step 312, the method 300 recites processing the one or more feedback signals and generating a test report. At step 314, the method 300 recites sharing the generated test report with a host computing device 104.

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[0046] The method 300 further comprises adjusting the one or more signals provided to the plurality of control units 112 to control their operations, in response to the one or more feedback signals received by the simulation model 102. The method 300 further recites analysing the test report by host computing device 104 using a processing unit and displaying the test results based on the test report via a display unit.

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[0047] In this manner, a plurality of devices may be tested in an effective manner and at low cost, since the system comprises combination of various control units which may generate various test signals suitable for testing the plurality of device.

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[0048] According to an exemplary embodiment, the system disclosed in the present disclosure may be used for various test applications such as for testing an Energy Meter, a

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Blood Cell Counter, Offboard Charger (EVSE) and Battery Management System (BMS), but not limited thereto.

5 [0049] According to another exemplary embodiment, for testing the Offboard Charger (EVSE), the various control units such as ADC unit, DAC unit, Resistance unit, pulse generation unit (PWM) may be used to generate test signals and LIN interface, CAN interface and USB may be used for communicating signals between the DUT, simulation model and host computing device. Detailed structure of these units is shown in fig. 4. Further, the I/Os may be configured as shown in fig. 5.

10 [0050] The illustrated steps are set out to explain the exemplary embodiments shown, and it should be anticipated that ongoing technological development will change the manner in which particular functions are performed. These examples are presented herein for purposes of illustration, and not limitation. Further, the boundaries of the functional building blocks have
15 been arbitrarily defined herein for the convenience of the description. Alternative boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

20 [0051] Alternatives (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternatives fall within the scope and spirit of the disclosed embodiments.

25 [0052] Furthermore, one or more computer-readable storage media may be utilized in implementing embodiments consistent with the present disclosure. A computer-readable storage medium refers to any type of physical memory on which information or data readable by a processor may be stored. Thus, a computer-readable storage medium may store instructions for execution by one or more processors, including instructions for causing the processor(s) to perform steps or stages consistent with the embodiments described herein. The
30 term “computer- readable medium” should be understood to include tangible items and exclude carrier waves and transient signals, i.e., are non-transitory. Examples include random access memory (RAM), read-only memory (ROM), volatile memory, non-volatile memory, hard drives, CD ROMs, DVDs, flash drives, disks, and any other known physical storage media.

[0053] Suitable processors/controllers include, by way of example, a general purpose processor, a special purpose processor, a conventional processor, a digital signal processor (DSP), a plurality of microprocessors, one or more microprocessors in association with a DSP core, a controller, a microcontroller, Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs) circuits, any other type of integrated circuit (IC), and/or a state machine.

WE CLAIM:

1. A system for testing a plurality of devices, the system comprising:
 - a simulation model configured to simulate a test environment for a device under test (DUT) using a plurality of test signals, wherein said simulation model comprises a plurality of control units configured to generate the plurality of test signals based on the type of DUT;
 - a host computing device operatively coupled to the simulation model, wherein said host computing device is configured to:
 - provide one or more signals to operate the plurality of control units, on the basis of the type of DUT, so as to allow the simulation model to generate the plurality of test signals; and
 - configure a plurality of input/output (I/O) ports based on the simulated test environment;
 - an interface unit comprising the plurality of I/O ports, said I/O ports being configured to:
 - transmit the plurality of generated test signals to the DUT via a plurality of communication channels; and
 - receive one or more feedback signals from the DUT, via the plurality of communication channels, in response to transmitting the plurality of test signals; and
 - a microcontroller operatively coupled with the simulation model, said microcontroller is configured to:
 - process the one or more feedback signals and generate a test report; and
 - share the generated test report with the host computing device.
2. The system as claimed in claim 1, wherein the plurality of control units comprise:
 - a power control unit to generate controlled power signals for testing the DUT;
 - a resistance controlling unit to generate resistive signals for testing the DUT;
 - a pulse generation unit to generate modulated pulse signals for testing the DUT;and
 - a convertor unit comprising an analog to digital (ADC) converter to convert analog signals into digital signals and a digital to analog (DAC) converter to convert digital signals into analog signals.

3. The system as claimed in claim 1, wherein
 - the host computing device is further configured to adjust the one or more signals provided to the plurality of control units to control their operations, in response to the one or more feedback signals received by the simulation model.
4. The system as claimed in claim 1, wherein the host computing device further comprises:
 - a processing unit configured to analyse the received test report ; and
 - a display unit configured to display the test results based on the test report.
5. The system as claimed in claim 1, wherein the simulation model is configured to communicate with the host computing unit via a serial communication port.
6. The system as claimed in claim 1, wherein the host computing device comprises plurality of
 - APIs configured to:
 - control the operations of plurality of I/O ports; and
 - regulate the one or more signals to the plurality of control units.
7. The system as claimed in claim 1, wherein the simulation model further comprises:
 - a plurality of switches;
 - a power switching unit; and
 - a relay control unit.
8. A method for testing a device, comprising:
 - providing one or more signals to operate a plurality of control units of a simulation model, on the basis of the type of a device under test (DUT), to allow the simulation model to generate a plurality of test signals;
 - simulating a test environment for the DUT using the plurality of test signals;
 - configuring a plurality of input/output (I/O) ports based on the simulated test environment;
 - transmitting the plurality of generated test signals to the DUT via a plurality of communication channels;
 - receiving one or more feedback signals from the DUT, via the plurality of communication channels, in response to transmitting the plurality of test signals;

processing the one or more feedback signals and generating a test report; and sharing the generated test report with a host computing device.

9. The method as claimed in claim 8, further comprising:
adjusting the one or more signals provided to the plurality of control units to control their operations, in response to the one or more feedback signals received by the simulation model.
10. The method as claimed in claim 8, further comprising:
analysing the test report; and
displaying the test results based on the test report.

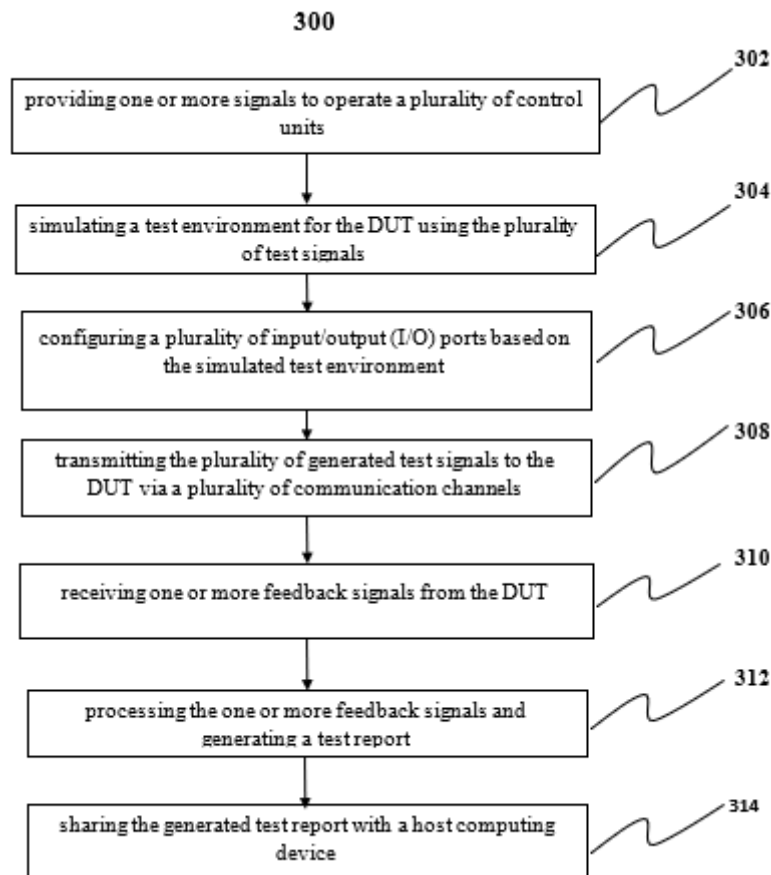
Dated this 11th day of October 2022

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ABSTRACT

SYSTEM AND METHOD FOR TESTING DEVICES

The present invention relates a system and method for testing plurality of devices. The method recites providing one or more signals to operate a plurality of control units of a simulation model, on the basis of the type of DUT, to allow the simulation model to generate plurality of test signals. The method recites simulating a test environment for the DUT using the test signals. The method further comprises configuring a plurality of I/O ports based on the simulated test environment. Further, the method comprises transmitting the generated test signals to the DUT via a plurality of communication channels and receiving feedback signals from the DUT, via the plurality of communication channels, in response to transmitting the plurality of test signals. Furthermore, the method comprises processing the feedback signals and generating a test report and sharing the generated test report with a host computing device.



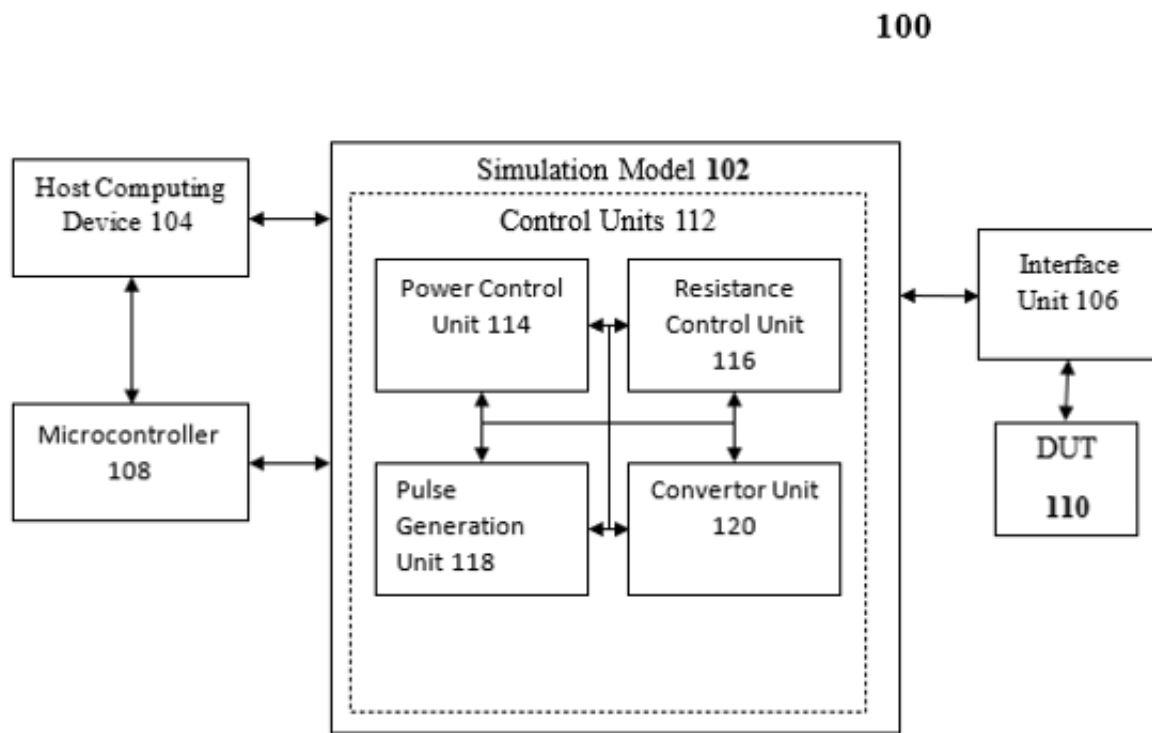


Fig. 1

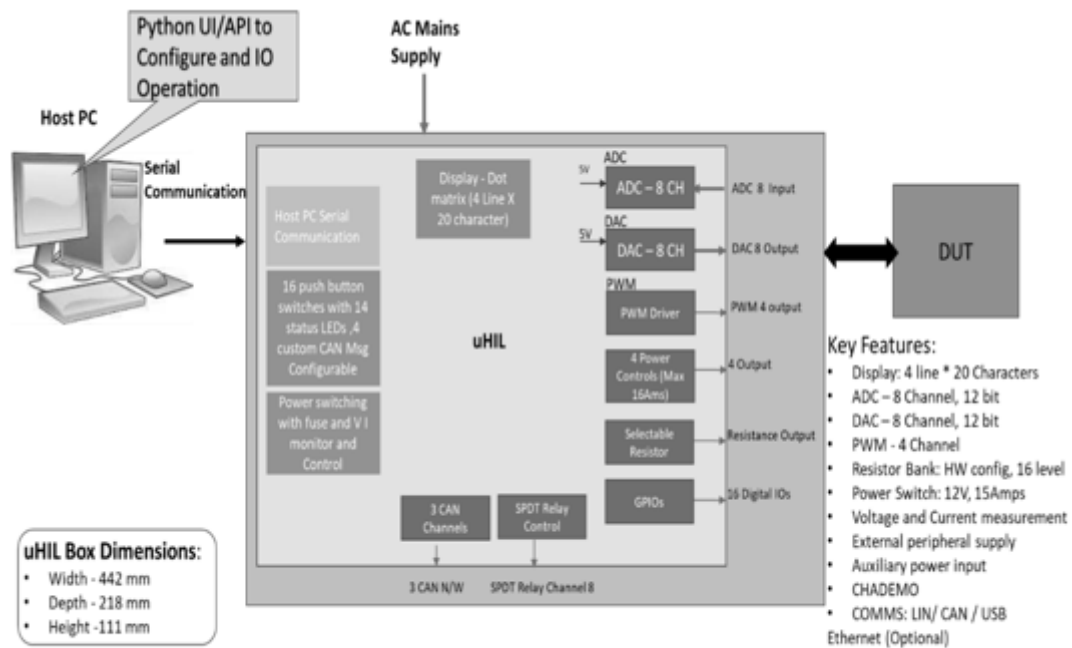


Fig. 2

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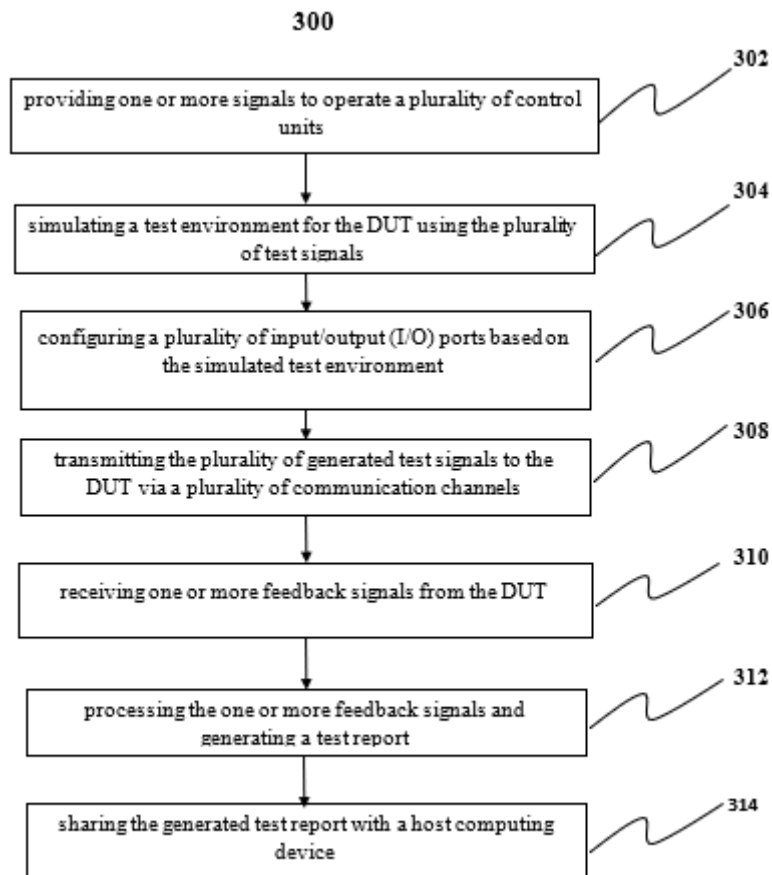


Fig. 3

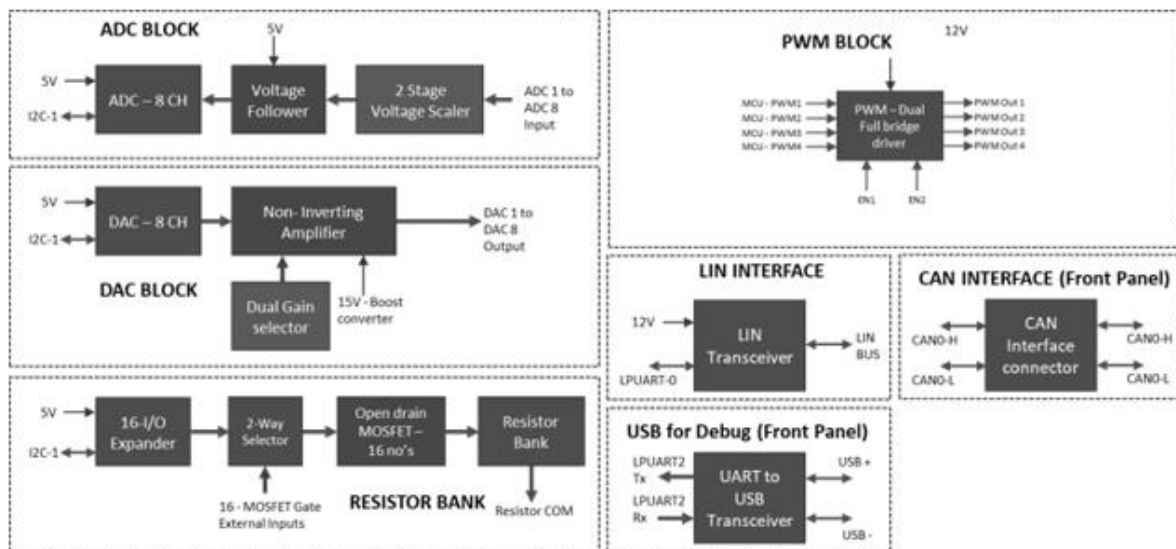


Fig. 4

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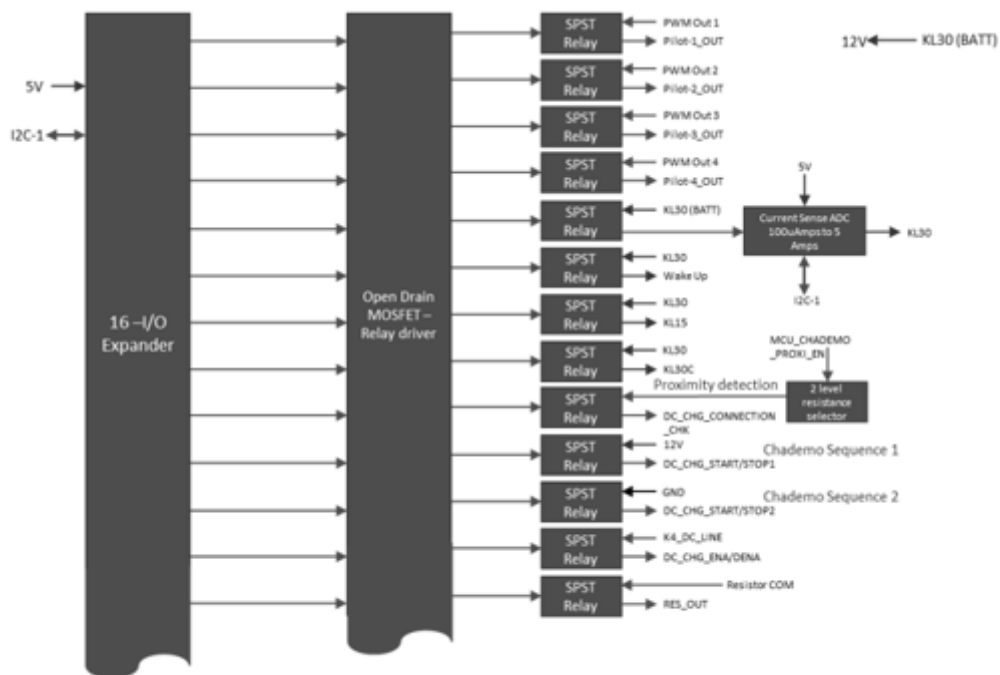


Fig. 5

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